

# OKI Semiconductor

1A

## MR27V1602D

1,048,576-Word x 16-Bit or 2,097,152-Word x 8-Bit  
Production Programmed Read Only Memory (P2ROM)

### DESCRIPTION

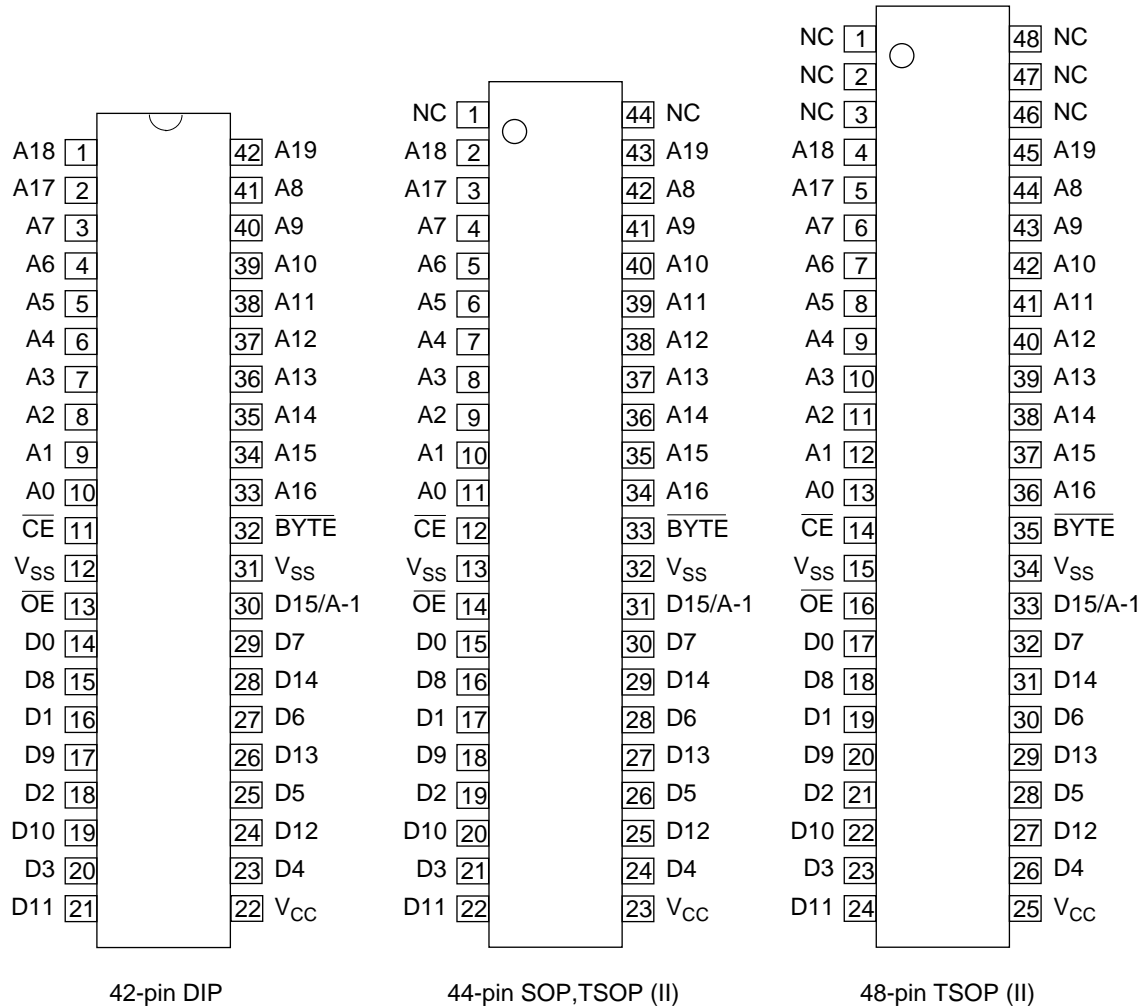
The MR27V1602D is a 16Mbit Production Programmed Read-Only Memory (P2ROM) whose configuration can be electrically switched between 1,048,576 word x 16bit and 2,097,152 word x 8 bit. The MR27V1602D operates on a single +3V-3.3V power supply and is TTL compatible. Since the MR27V1602D operates asynchronously, external clocks are not required, making this device easy-to-use. The MR27V1602D is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS double silicon gate technology and is offered in 42-pin DIP, 44-pin SOP, 44-pin TSOP or 48-pin TSOP packages.

### FEATURES

- 1,048,576 word x 16bit / 2,097,152 word x 8bit electrically switchable configuration
- Single +3V-3.3V power supply
- Access time                   90ns access time ( $V_{cc}=+3V$ )  
   80ns access time ( $V_{cc}=+3.3V$ )
- Input / Output TTL compatible
- Three-state output
- Packages

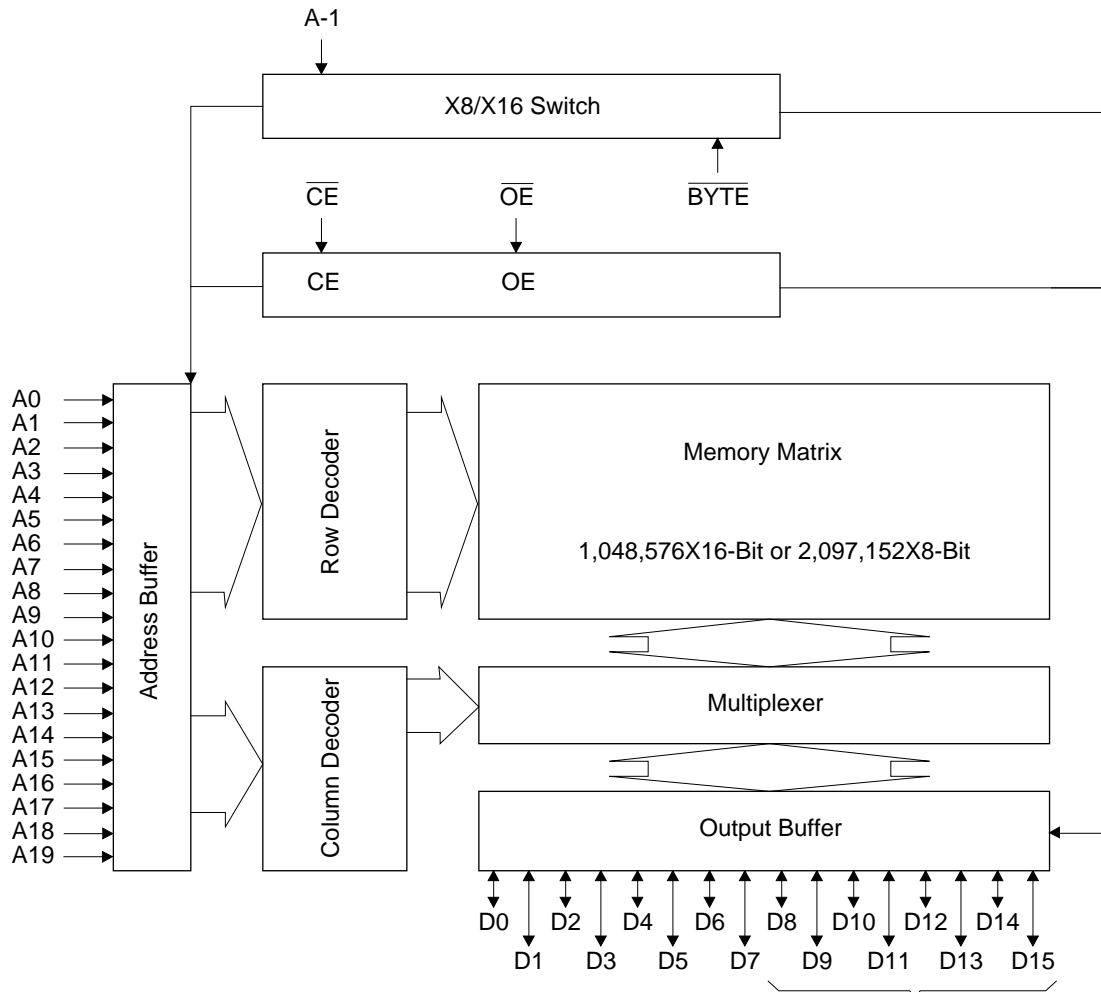
42-pin plastic DIP (DIP42-P-600-2.54)                   (Product name : MR27V1602D-xxRA)  
44-pin plastic SOP (SOP44-P-600-1.27-K)           (Product name : MR27V1602D-xxMA)  
44-pin plastic TSOP (TSOP II 44-P-400-0.80-K)   (Product name : MR27V1602D-xxTP)  
48-pin plastic TSOP (TSOP II 48-P-550-0.80-K)   (Product name : MR27V1602D-xxTA)

## PIN CONFIGURATION (TOP VIEW)



PIN NAMES	FUNCTIONS
D15/A-1	Data output / Address input
A0-A19	Address input
D0-D14	Data output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$V_{CC}$	Power supply voltage
$V_{SS}$	GND
BYTE	Mode switch
NC	Non connection

## BLOCK DIAGRAM



In 8-bit output mode, these pins are three-stated and pin D15 functions as the A-1 address pin.

## FUNCTION TABLE

MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{BYTE}}$	$V_{\text{CC}}$	D0 - D7	D8 - D14	D15/A-1
READ (16-Bit)	L	L	H	3.0V to 3.3V	$D_{\text{OUT}}$		
READ (8-Bit)	L	L	L		$D_{\text{OUT}}$	Hi-Z	L/H
OUTPUT DISABLE	L	H	H		Hi-Z		*
			L		Hi-Z		*
STAND-BY	H	*	H	Hi-Z		*	
			L	Hi-Z		*	

\*: Don't Care

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	$T_{opr}$	-	0 to 70	°C
Storage temperature	$T_{stg}$		-55 to 125	°C
Input voltage	$V_I$	relative to $V_{SS}$	-0.5 to $V_{CC} + 0.5$	V
Output voltage	$V_O$		-0.5 to $V_{CC} + 0.5$	V
Power supply voltage	$V_{CC}$		-0.5 to 5	V
Power dissipation per package	$P_D$	-	1.0	W

**RECOMMENDED OPERATING CONDITIONS**

(Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
$V_{CC}$ power supply voltage	$V_{CC}$	$V_{CC}=2.7V-3.6V$	2.7	-	3.6	V
Input "H" level	$V_{IH}$		2.2	-	$V_{CC}+0.5^*$	V
Input "L" level	$V_{IL}$		-0.5**	-	0.6	V

Voltage is relative to  $V_{SS}$ \* :  $V_{CC}+1.5V$  (Max.) when pulse width of overshoot is less than 10nS.

\*\* : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

**ELECTRICAL CHARACTERISTICS (Read operation)****DC Characteristics 1**(V<sub>CC</sub>=3V±0.3V, T<sub>a</sub>=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I <sub>LI</sub>	V <sub>I</sub> =0 to V <sub>CC</sub>	-	-	10	μA
Output leakage current	I <sub>LO</sub>	V <sub>O</sub> =0 to V <sub>CC</sub>	-	-	10	μA
V <sub>CC</sub> power supply current (Standby)	I <sub>CCSC</sub>	$\overline{CE}=V_{CC}$	-	-	50	μA
	I <sub>CCST</sub>	$\overline{CE}=V_{IH}$	-	-	1	mA
V <sub>CC</sub> power supply current (Read)	I <sub>CCA</sub>	$\overline{CE}=V_{IL}, \overline{OE}=V_{IH}$ tc=90ns	-	-	35	mA
Input "H" level	V <sub>IH</sub>	-	2.2	-	V <sub>CC</sub> +0.5*	V
Input "L" level	V <sub>IL</sub>	-	-0.5**	-	0.6	V
Output "H" level	V <sub>OH</sub>	I <sub>OH</sub> =-400uA	2.4	-	-	V
Output "L" level	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V

Voltage is relative to V<sub>SS</sub>\* : V<sub>CC</sub>+1.5V (Max.) when pulse width of overshoot is less than 10nS.

\*\* : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

**DC Characteristics 2**(V<sub>CC</sub>=3.3V±0.3V, T<sub>a</sub>=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I <sub>LI</sub>	V <sub>I</sub> =0 to V <sub>CC</sub>	-	-	10	μA
Output leakage current	I <sub>LO</sub>	V <sub>O</sub> =0 to V <sub>CC</sub>	-	-	10	μA
V <sub>CC</sub> power supply current (Standby)	I <sub>CCSC</sub>	$\overline{CE}=V_{CC}$	-	-	50	μA
	I <sub>CCST</sub>	$\overline{CE}=V_{IH}$	-	-	1	mA
V <sub>CC</sub> power supply current (Read)	I <sub>CCA</sub>	$\overline{CE}=V_{IL}, \overline{OE}=V_{IH}$ tc=80ns	-	-	40	mA
Input "H" level	V <sub>IH</sub>	-	2.2	-	V <sub>CC</sub> +0.5*	V
Input "L" level	V <sub>IL</sub>	-	-0.5**	-	0.6	V
Output "H" level	V <sub>OH</sub>	I <sub>OH</sub> =-400uA	2.4	-	-	V
Output "L" level	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V

Voltage is relative to V<sub>SS</sub>\* : V<sub>CC</sub>+1.5V (Max.) when pulse width of overshoot is less than 10nS.

\*\* : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

**AC Characteristics 1**(V<sub>CC</sub>=3V±0.3V, Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	T <sub>C</sub>	-	90	-	ns
Address access time	T <sub>ACC</sub>	$\overline{CE}=\overline{OE}=V_{IL}$	-	90	ns
$\overline{CE}$ access time	T <sub>CE</sub>	$\overline{OE}=V_{IL}$	-	90	ns
$\overline{OE}$ access time	T <sub>OE</sub>	$\overline{CE}=V_{IL}$	-	45	ns
Output disable time	T <sub>CHZ</sub>	$\overline{OE}=V_{IL}$	0	30	ns
	T <sub>OHZ</sub>	$\overline{CE}=V_{IL}$	0	25	ns
Output hold time	T <sub>OH</sub>	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

## Measurement conditions

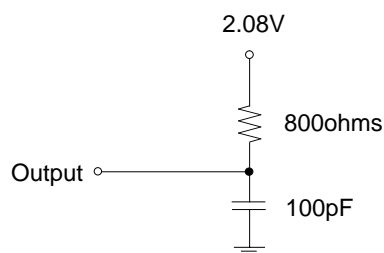
Input signal level	-----	0V/3V
Input timing reference level	-----	0.8V/2.0V
Output load	-----	100pF
Output timing reference level	-----	0.8V/2.0V

**AC Characteristics 2**(V<sub>CC</sub>=3.3V±0.3V, Ta=0 to 70°C)

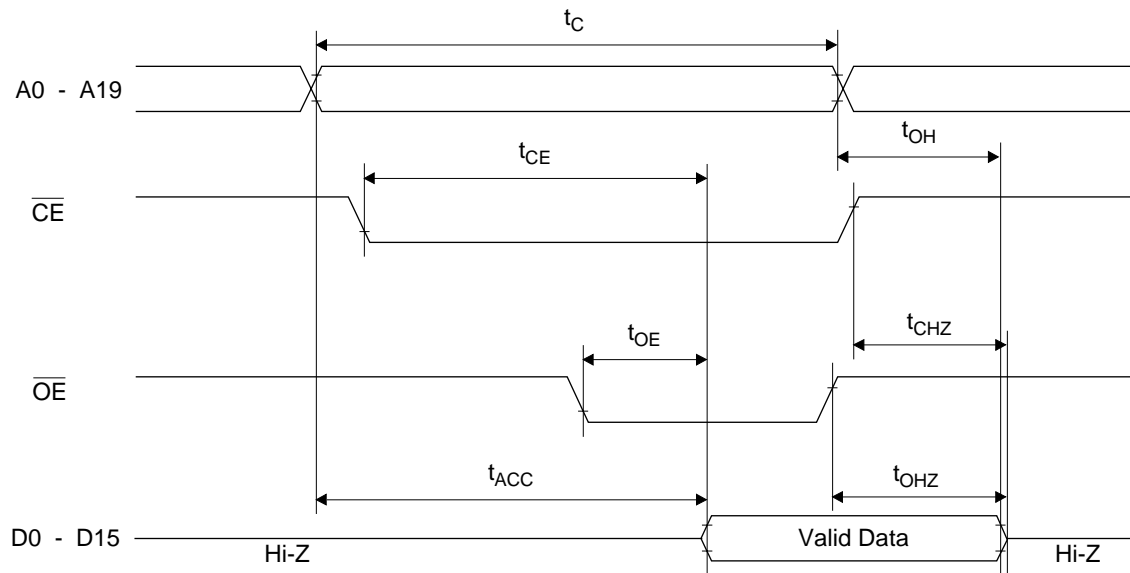
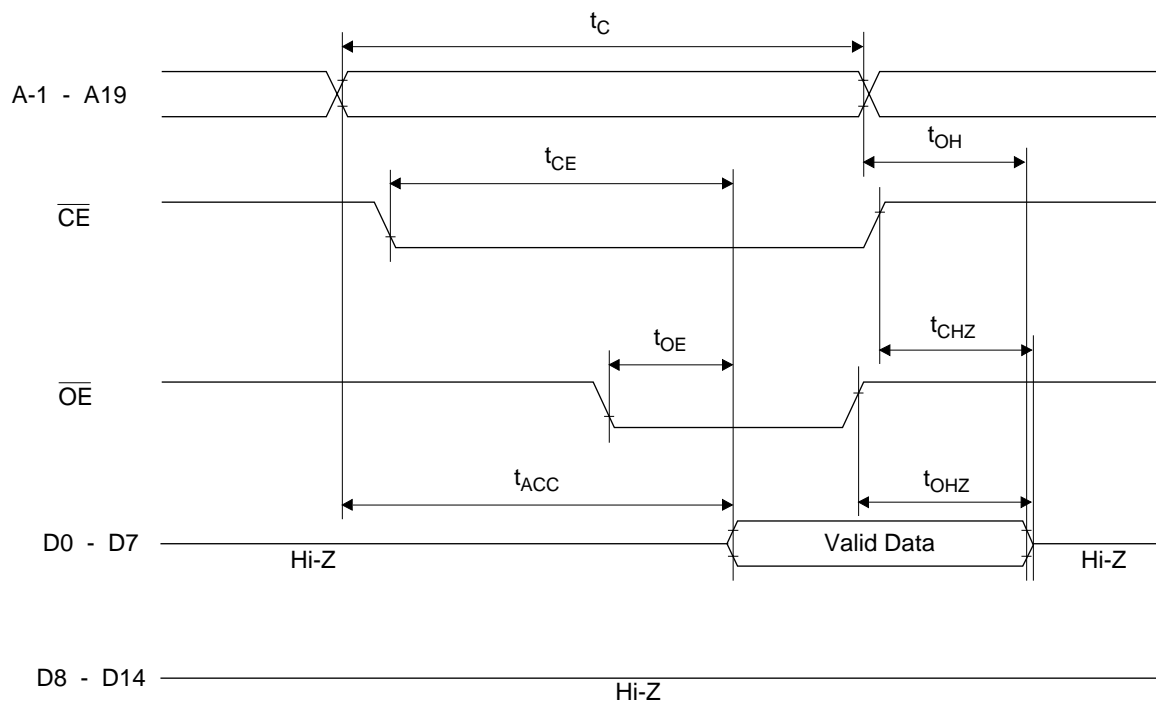
Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	T <sub>C</sub>	-	80	-	ns
Address access time	T <sub>ACC</sub>	$\overline{CE}=\overline{OE}=V_{IL}$	-	80	ns
$\overline{CE}$ access time	T <sub>CE</sub>	$\overline{OE}=V_{IL}$	-	80	ns
$\overline{OE}$ access time	T <sub>OE</sub>	$\overline{CE}=V_{IL}$	-	40	ns
Output disable time	T <sub>CHZ</sub>	$\overline{OE}=V_{IL}$	0	30	ns
	T <sub>OHZ</sub>	$\overline{CE}=V_{IL}$	0	25	ns
Output hold time	T <sub>OH</sub>	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

## Measurement conditions

Input signal level	-----	0V/3V
Input timing reference level	-----	0.8V/2.0V
Output load	-----	100pF
Output timing reference level	-----	0.8V/2.0V



## TIMING CHART (READ CYCLE)

16-Bit Read Mode ( $\overline{\text{BYTE}}=\text{V}_{\text{IH}}$ )8-Bit Read Mode ( $\overline{\text{BYTE}}=\text{V}_{\text{IL}}$ )

**PIN Capacitance**(V<sub>CC</sub>=3.3V, T<sub>a</sub>=25°C, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C <sub>IN1</sub>	V <sub>I</sub> =0V	-	-	8 (10)	pF
$\overline{\text{BYTE}}$	C <sub>IN2</sub>		-	-	120	
Output	C <sub>OUT</sub>	V <sub>O</sub> =0V	-	-	10 (12)	

( ) : DIP only