

OKI Semiconductor

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MR27V3252D

2,097,152-Word x 16-Bit or 4,194,304-Word x 8-Bit

8-Word x 16-Bit or 16-Word x 8-Bit Page Mode

Production Programmed Read Only Memory (P2ROM)

DESCRIPTION

The MR27V3252D is a 32Mbit Production Programmed Read-Only Memory (P2ROM) with page mode. Its configuration can be electrically switched between 2,097,152 word x 16bit and 4,194,304 word x 8bit. The MR27V3252D operates on a single +3.3V power supply and is TTL compatible. The MR27V3252D provides Page mode which can greatly reduce the read access time. Since the MR27V3252D operates asynchronously, external clocks are not required, making this device easy-to-use. The MR27V3252D is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS double silicon gate technology and is offered in 44-pin SOP or 48-pin TSOP packages.

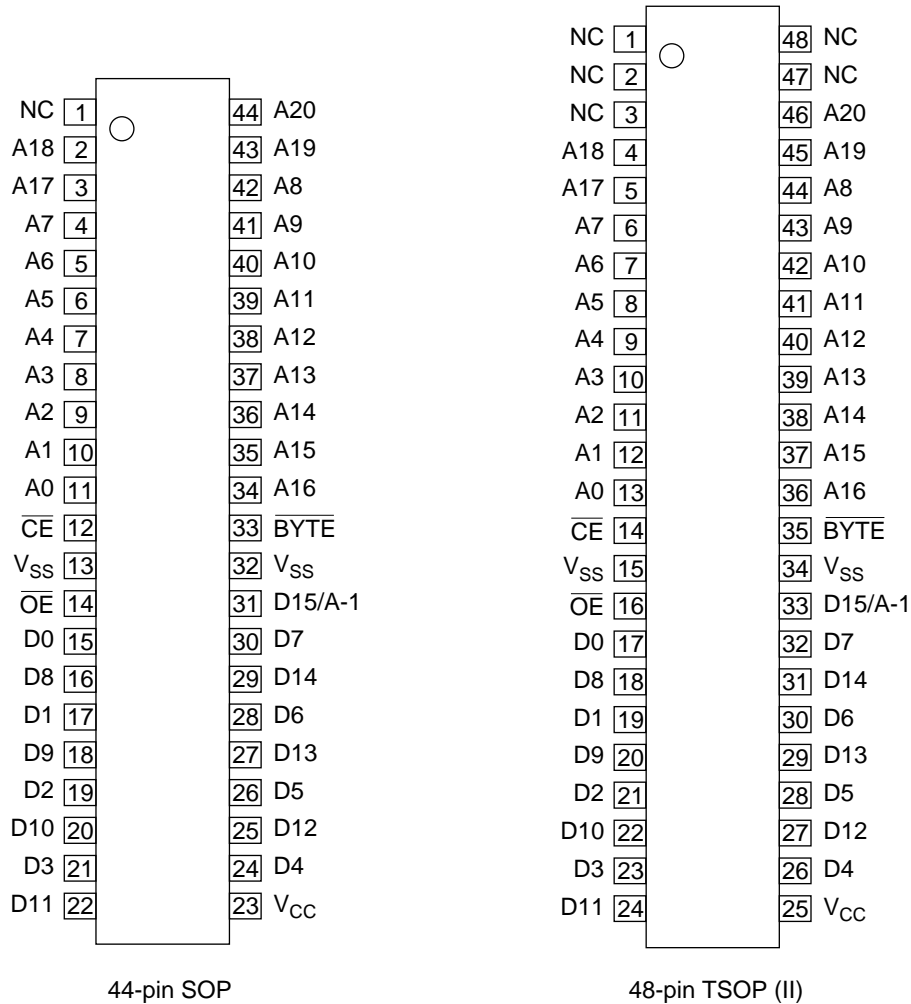
FEATURES

- 2,097,152 word x 16bit / 4,194,304 word x 8bit electrically switchable configuration
- Single +3.3V power supply
- Access time 100ns
Page mode access time 30ns
- Input / Output TTL compatible
- Three-state output
- Packages

44-pin plastic SOP (SOP44-P-600-1.27-K) (Product name : MR27V3252D-xxMA)

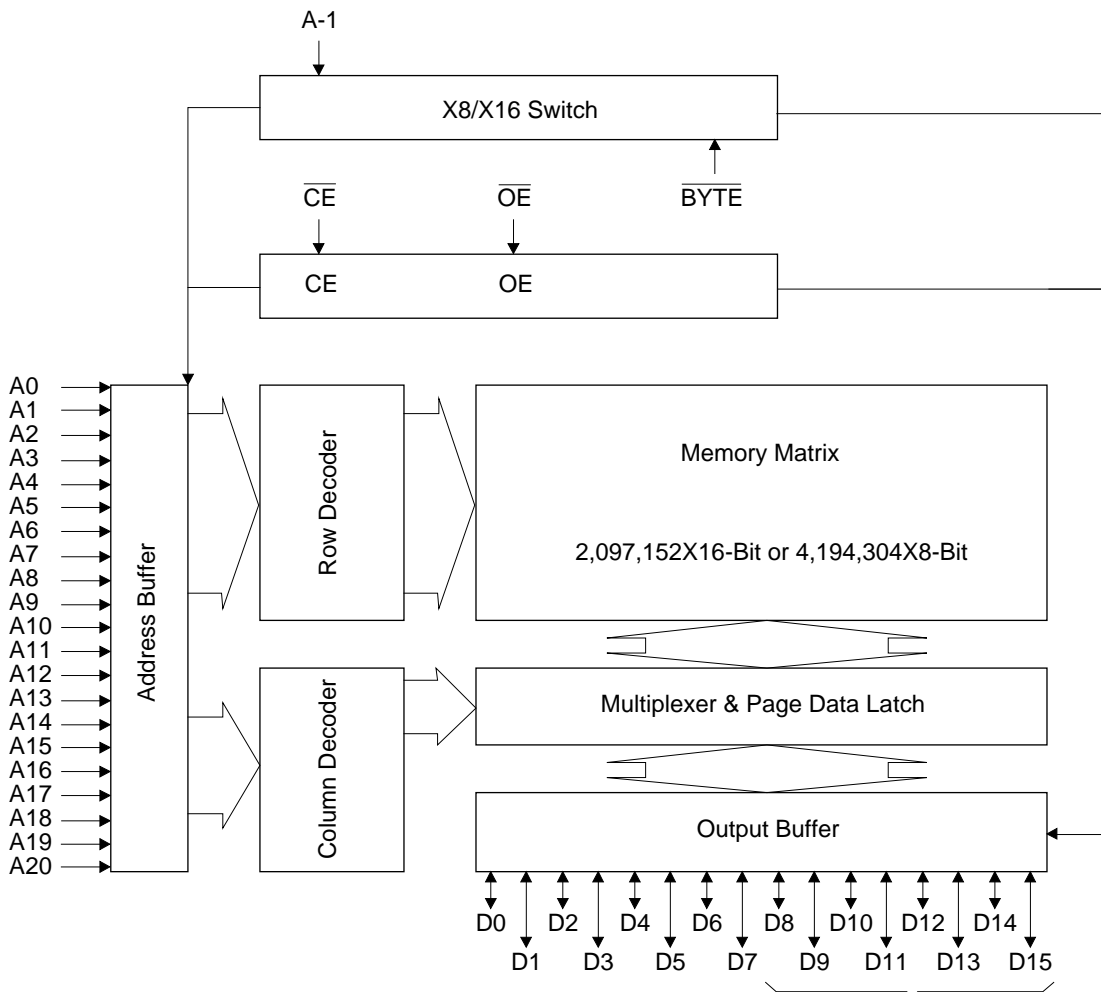
48-pin plastic TSOP (TSOP II 48-P-550-0.80-K) (Product name : MR27V3252D-xxTA)

PIN CONFIGURATION (TOP VIEW)



PIN NAMES	FUNCTIONS
D15/A-1	Data output / Address input
A0 - A20	Address input
D0 - D14	Data output
\overline{CE}	Chip enable
\overline{OE}	Output enable
V_{CC}	Power supply voltage
V_{SS}	GND
\overline{BYTE}	Mode switch
NC	Non connection

BLOCK DIAGRAM



In 8-bit output mode, these pins are three-stated and pin D15 functions as the A-1 address pin.

FUNCTION TABLE

MODE	\overline{CE}	\overline{OE}	\overline{BYTE}	V_{CC}	D0 - D7	D8 - D14	D15/A-1
READ (16-Bit)	L	L	H	3.3V	D_{OUT}		
READ (8-Bit)	L	L	L		D_{OUT}	Hi-Z	L/H
OUTPUT DISABLE	L	H	H		Hi-Z		*
			L		Hi-Z		*
STAND-BY	H	*	H	Hi-Z		*	
			L	Hi-Z		*	

* : Don't Care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T_{opr}	-	0 to 70	°C
Storage temperature	T_{stg}		-55 to 125	°C
Input voltage	V_I	relative to V_{SS}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_O		-0.5 to $V_{CC} + 0.5$	V
Power supply voltage	V_{CC}		-0.5 to 5	V
Power dissipation per package	P_D	-	1.0	W

RECOMMENDED OPERATING CONDITIONS FOR READ

(Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{CC} power supply voltage	V_{CC}	$V_{CC}=3.0V-3.6V$	3.0	-	3.6	V
Input "H" level	V_{IH}		2.2	-	$V_{CC}+0.5^*$	V
Input "L" level	V_{IL}		-0.5**	-	0.6	V

Voltage is relative to V_{SS} * : $V_{CC}+1.5V$ (Max.) when pulse width of overshoot is less than 10nS.

** : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

ELECTRICAL CHARACTERISTICS (Read operation)**DC Characteristics** $(V_{CC}=3.3V\pm 0.3V, T_a=0 \text{ to } 70^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	$V_I=0 \text{ to } V_{CC}$	-	-	10	μA
Output leakage current	I_{LO}	$V_O=0 \text{ to } V_{CC}$	-	-	10	μA
V_{CC} power supply current (Standby)	I_{CS1}	$\overline{CE}=V_{CC}$	-	-	50	μA
	I_{CS2}	$\overline{CE}=V_{IH}$	-	-	1	mA
V_{CC} power supply current (Read)	I_{CCA}	$\overline{CE}=V_{IL}, \overline{OE}=V_{IH}$ $t_c=100\text{ns}$	-	-	100	mA
Input "H" level	V_{IH}	-	2.2	-	$V_{CC}+0.5^*$	V
Input "L" level	V_{IL}	-	-0.5**	-	0.6	V
Output "H" level	V_{OH}	$I_{OH}=-400\mu\text{A}$	2.4	-	-	V
Output "L" level	V_{OL}	$I_{OL}=2.1\text{mA}$	-	-	0.4	V

Voltage is relative to V_{SS} * : $V_{CC}+1.5\text{V}$ (Max.) when pulse width of overshoot is less than 10nS.

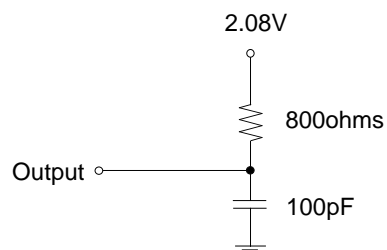
** : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

AC Characteristics $(V_{CC}=3.3V\pm 0.3V, T_a=0 \text{ to } 70^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Max.	Unit
Address access cycle time	T_C	-	100	-	ns
Address access time	T_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	-	100	ns
Page access cycle time	T_{PC}	-	30	-	ns
Page access time	T_{PAC}	-	-	30	ns
\overline{CE} access time	T_{CE}	$\overline{OE}=V_{IL}$	-	100	ns
\overline{OE} access time	T_{OE}	$\overline{CE}=V_{IL}$	-	40	ns
Output disable time	T_{CHZ}	$\overline{OE}=V_{IL}$	0	30	ns
	T_{OHZ}	$\overline{CE}=V_{IL}$	0	25	ns
Output hold time	T_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

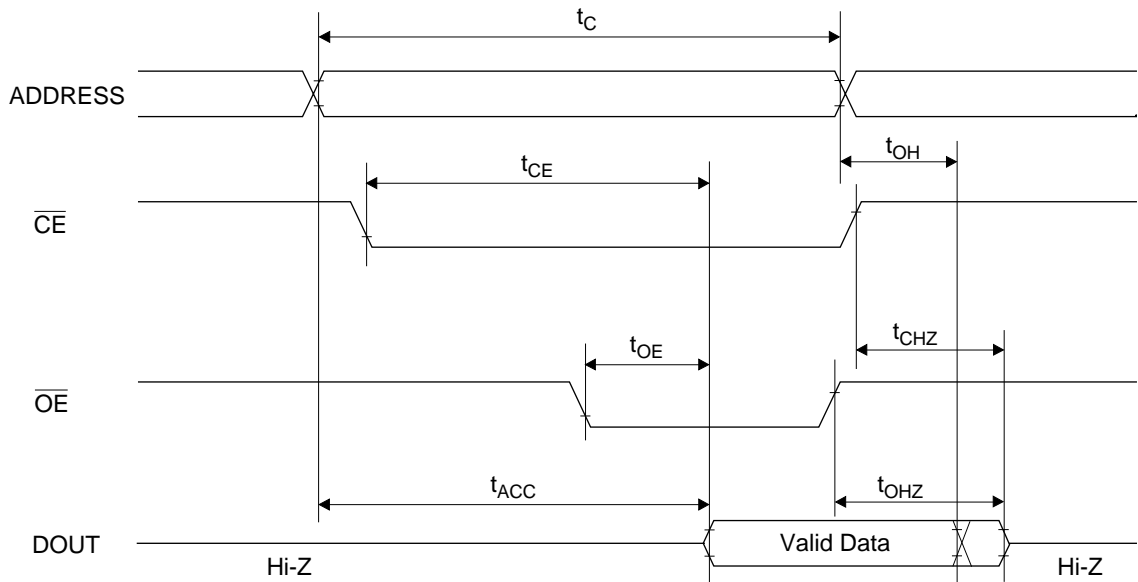
Measurement conditions

Input signal level	-----	0V/3V
Input timing reference level	-----	0.8V/2.0V
Output load	-----	100pF
Output timing reference level	-----	0.8V/2.0V

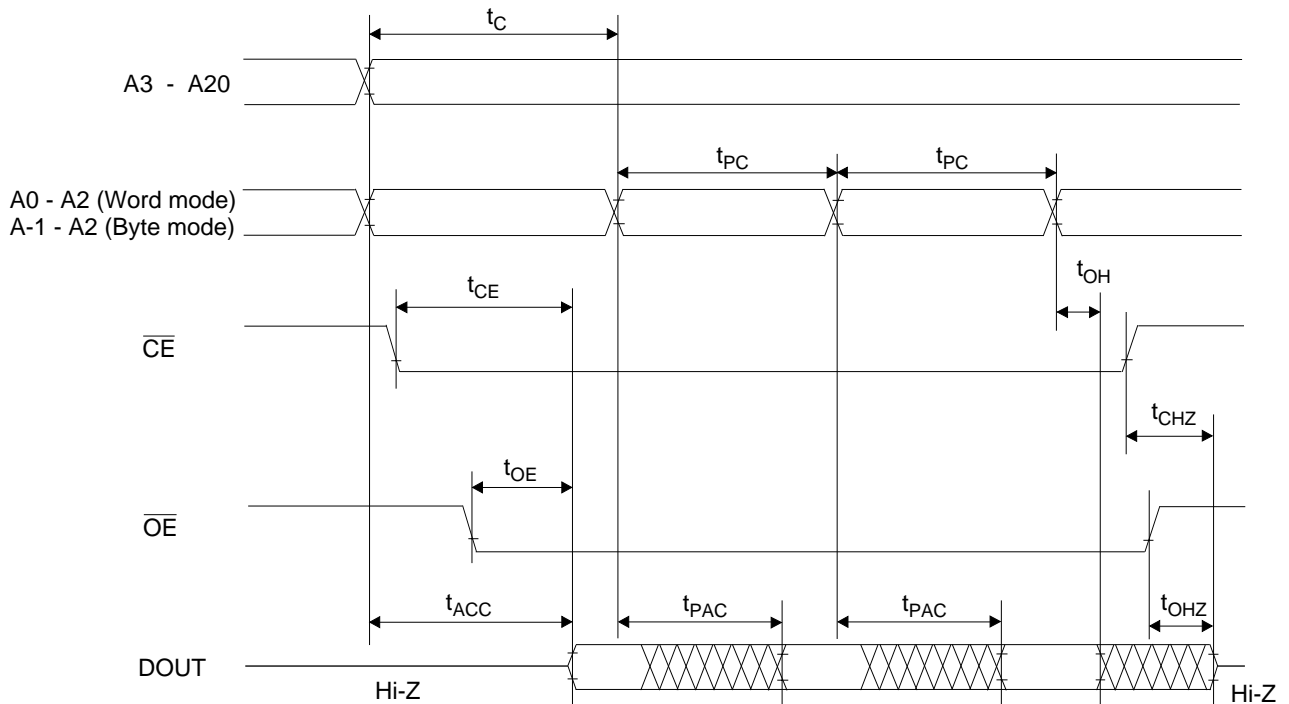


TIMING CHART

NORMAL MODE READ CYCLE



PAGE MODE READ CYCLE



PIN Capacitance $(V_{CC}=3.3V, T_a=25^{\circ}C, f=1MHz)$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C_{IN1}	$V_I=0V$	-	-	8	pF
\overline{BYTE}	C_{IN2}		-	-	120	
Output	C_{OUT}	$V_O=0V$	-	-	10	