

## MS52C181A

## Preliminary

131,072-Word X 8-Bit STATIC RAM +  
1,048,576-Word X 8-Bit One Time PROM

### DESCRIPTION

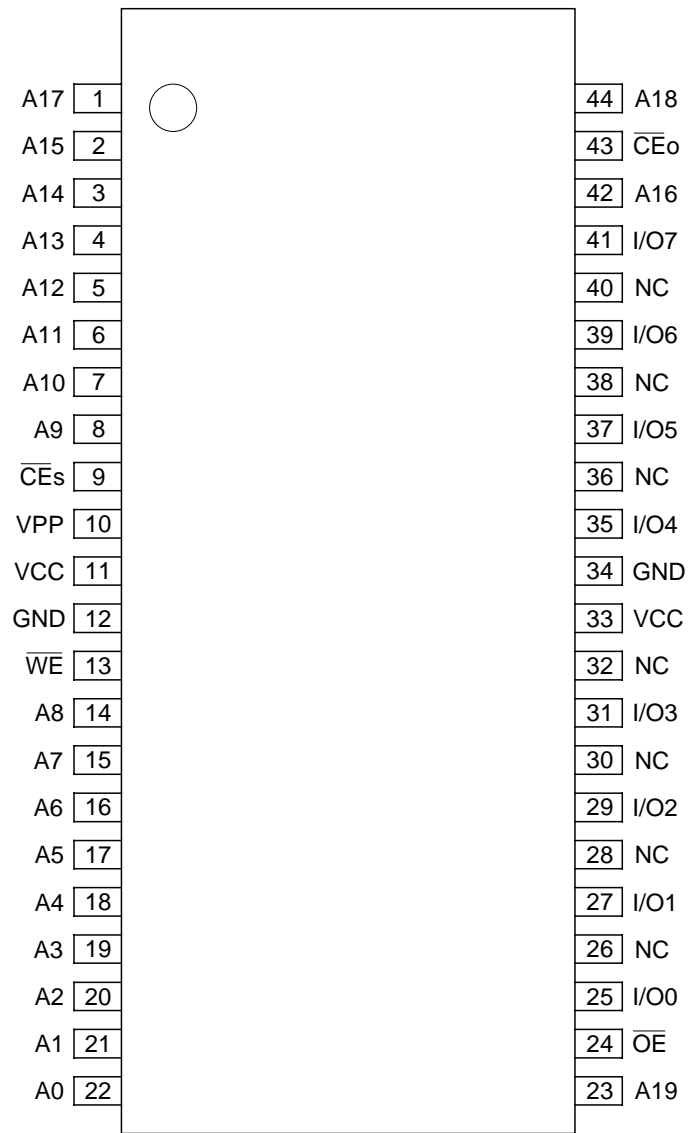
The MS52C181A is a 131,072-word by 8-bit electrically switchable 1Mb static RAM and 1,048,576-word by 8-bit electrically switchable 8Mb One Time PROM featuring 2.7V to 3.6V power supply operation and direct LVTTTL input / output compatibility. Since the circuitry is completely static, external clocks are unnecessary, making this device very easy to use. The MS52C181A is packaged in 44-pin plastic TSOP and 48-pin FBGA (9mmx10mm), suited for use in handy terminal and other application which required small space.

### FEATURES

- 131,072-word x 8-bit configuration SRAM and 1,048,576-word x 8-bit configuration OTP
- Power supply voltage : 2.7 to 3.6V
- Fully static operation
- Operating temperature range : Ta= -20 to 70°C
- Access time : 100nS MAX (Vcc=2.7V)  
80nS MAX (Vcc=3.0V)
- Common address inputs and data inputs / outputs for SRAM and OTP
- Input / Output LVTTTL compatible
- 3-state output
- Data retention available at power supply voltage 1.5V for SRAM
- Package options :

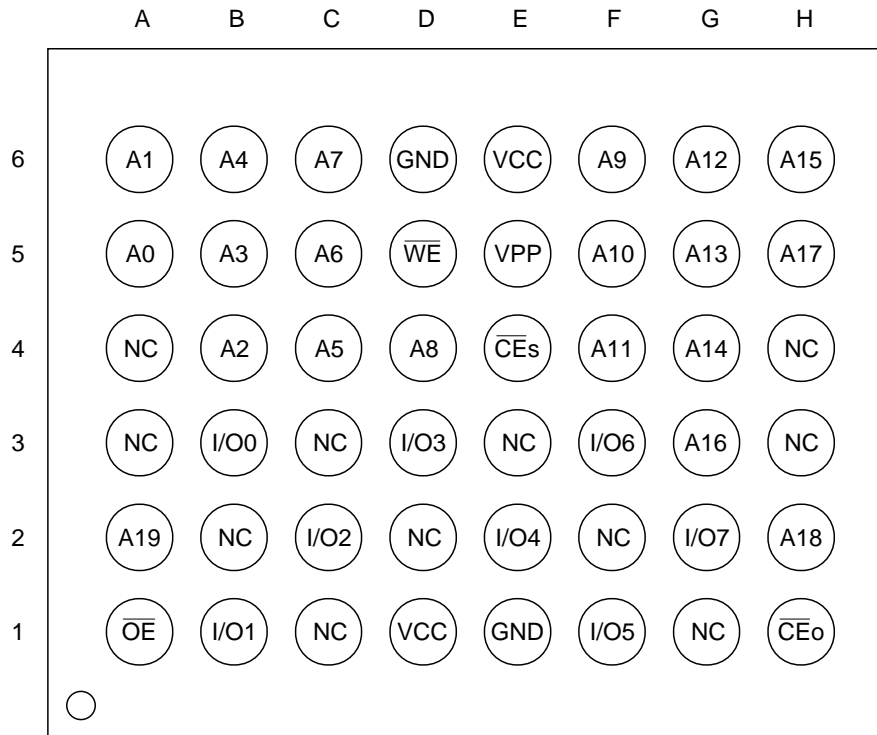
44-pin plastic TSOP (Type II)	(TSOP44-P-400-0.8)	(Product : MS52C181ATA)
48-pin plastic FBGA	(FBGA48-P-0910-0.8)	(Product : MS52C181ALA)

PIN CONFIGURATION (TOP VIEW)



44-pin TSOP (II)

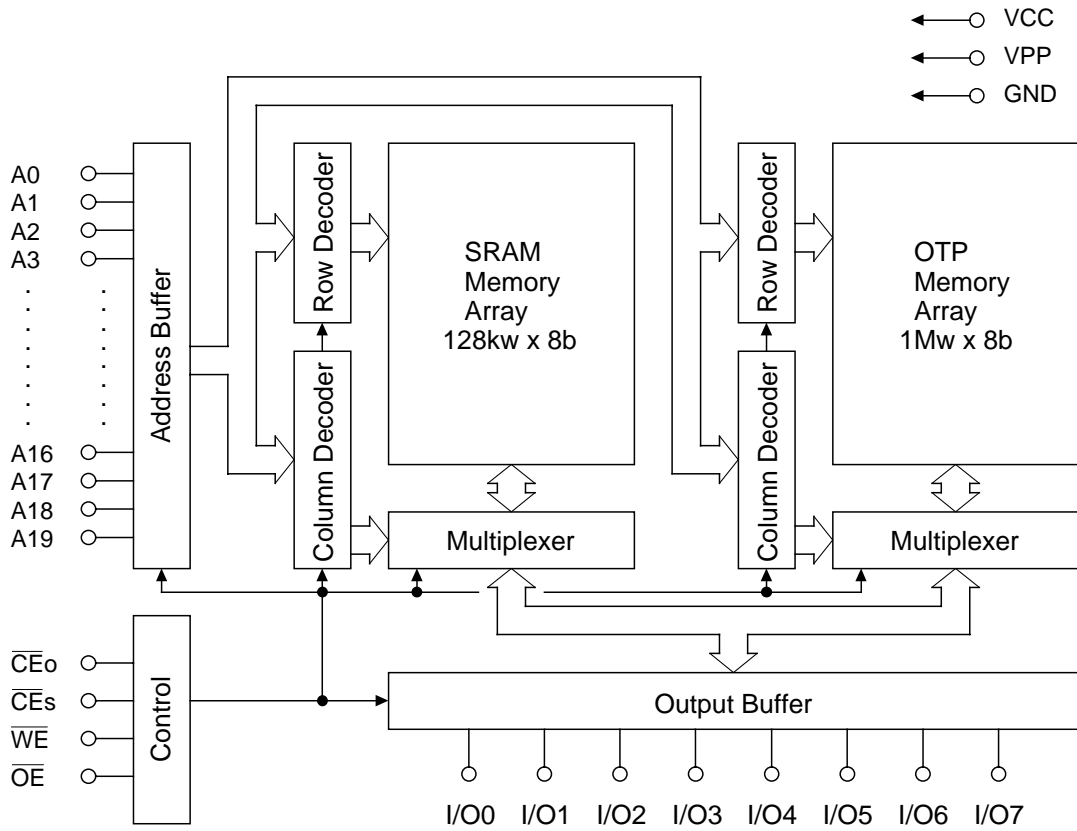
**PIN CONFIGURATION (TOP VIEW)**



48-pin FBGA

Pin Name	Function
A0 - A16	Common Address Inputs
A17 - A19	Address Inputs for OTP
$\overline{CEs}$	Chip Enable for SRAM
$\overline{CEo}$	Chip Enable for OTP
$\overline{WE}$	Write Enable for SRAM
$\overline{OE}$	Common Output Enable
I/O0 - I/O7	Common Data Inputs / Outputs
VCC	Common Power Supply
VPP	Program Power Supply for OTP
GND	Common Ground
NC	No Connection

**BLOCK DIAGRAM**



**FUNCTION TABLE**

Operating Mode	$\overline{CE}_o$	$\overline{CE}_s$	$\overline{WE}$	$\overline{OE}$	VPP	VCC	I/O0 to I/O7
Standby	H	H	*	*	*	2.7V to 3.6V	High-Z
SRAM Read	H	L	H	H	*		High-Z
	H	L	H	L	*		DOUT
SRAM Write	H	L	L	*	*		DIN
OTP Read	L	H	*	H	*	4.0V	High-Z
	L	H	*	L	*		DOUT
OTP Program	L	H	*	H	9.75V		DIN
OTP Program Inhibit	H	H	*	H			High-Z
OTP Program Verify	H	H	*	L		DOUT	

Note : 1. \* = Don't Care ("H" or "L")

2. It is forbidden to apply  $\overline{CE}_o$ ="L" and  $\overline{CE}_s$ ="L" simultaneously.

**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	VCC	Respect to GND	-0.5 to 5.0	V
	VPP		-0.5 to 11.5	V
Input Voltage	VI		-0.5* to Vcc+0.5	V
Output Voltage	VO		-0.5* to Vcc+0.5	V
Power Dissipation	PD	Ta=25°C	0.7	W
Operating Temperature	Topr	—	-20 to 70	°C
Storage Temperature	Tstg	—	-55 to 125	°C

\* -1.2VMin. for pulse width less than 30nS.

**Recommended Operating Conditions**

(Ta= -20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	VCC	—	2.7	—	3.6	V
	VPP		-0.5	—	Vcc+0.5	V
	GND		0	0	0	V
SRAM Data Retention Voltage	VCCH	—	1.5	—	3.6	V
Input High Voltage	VIH	Vcc=2.7 to 3.6	2.2	—	Vcc+0.5	V
Input Low Voltage	VIL		-0.5*	—	0.4	V

\* -1.2VMin. for pulse width less than 30nS.

**Capacitance**

(Vcc=3.3V , Ta=25°C , f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Capacitance	CIN	V I=0V	—	—	10	pF
Input/Output Capacitance	CI/O	VO=0V	—	—	10	pF

Note : This parameter is periodically sampled and not 100% tested.

## DC Characteristics (1)

(V<sub>CC</sub>=3.0V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =0 to V <sub>CC</sub>	-1.0	—	1.0	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CE}_o=V_{IH}$ , $\overline{CE}_s=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>OUT</sub> =0 to V <sub>CC</sub>	-1.0	—	1.0	μA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-500μA	V <sub>CC</sub> -0.5	—	—	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	—	—	0.4	V
Standby Power Supply Current	I <sub>CCS</sub>	$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ V <sub>IN</sub> =0 to V <sub>CC</sub>	—	—	10	μA
	I <sub>CCS1</sub>	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	—	—	0.3	mA
Operating Power Supply Current	I <sub>CCA</sub> (SRAM)	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IL}$ $\overline{OE}=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> /V <sub>IL</sub> T <sub>CYC</sub> =100nS	—	—	35	mA
		$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \leq 0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V V <sub>IL</sub> ≤ 0.2V T <sub>CYC</sub> =1μS	—	—	10	mA
	I <sub>CCA</sub> * (OTP)	$\overline{CE}_o=V_{IL}$ $\overline{CE}_s=V_{IH}$ $\overline{OE}=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> /V <sub>IL</sub> T <sub>CYC</sub> =100nS	—	—	35	mA
		$\overline{CE}_o \leq 0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V V <sub>IL</sub> ≤ 0.2V T <sub>CYC</sub> =1μS	—	—	20	mA
V <sub>PP</sub> Power Supply Current	I <sub>PP</sub>	V <sub>PP</sub> =V <sub>CC</sub>	—	—	10	μA

\* Read Current

## DC Characteristics (2)

(V<sub>CC</sub>=3.3V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =0 to V <sub>CC</sub>	-1.0	—	1.0	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CE}_o=V_{IH}$ , $\overline{CE}_s=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>OUT</sub> =0 to V <sub>CC</sub>	-1.0	—	1.0	μA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-500μA	V <sub>CC</sub> -0.5	—	—	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	—	—	0.4	V
Standby Power Supply Current	I <sub>CCS</sub>	$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ V <sub>IN</sub> =0 to V <sub>CC</sub>	—	—	10	μA
	I <sub>CCS1</sub>	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	—	—	0.3	mA
Operating Power Supply Current	I <sub>CCA</sub> (SRAM)	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IL}$ $\overline{OE}=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> /V <sub>IL</sub> TCYC=80nS	—	—	40	mA
		$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \leq 0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V V <sub>IL</sub> ≤ 0.2V TCYC=1μS	—	—	15	mA
	I <sub>CCA</sub> * (OTP)	$\overline{CE}_o=V_{IL}$ $\overline{CE}_s=V_{IH}$ $\overline{OE}=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> /V <sub>IL</sub> TCYC=80nS	—	—	40	mA
		$\overline{CE}_o \leq 0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V V <sub>IL</sub> ≤ 0.2V TCYC=1μS	—	—	25	mA
V <sub>PP</sub> Power Supply Current	I <sub>PP</sub>	V <sub>PP</sub> =V <sub>CC</sub>	—	—	10	μA

\* Read Current

**SRAM AC Characteristics**

**SRAM Read Cycle (1)**

(V<sub>CC</sub>=3.0V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t <sub>RC</sub>	—	100	—	nS
Address Access Time	t <sub>AA</sub>	—	—	100	nS
$\overline{C\!E}$ s Access Time	t <sub>CO</sub>	—	—	100	nS
$\overline{O\!E}$ Access Time	t <sub>OE</sub>	—	—	50	nS
$\overline{C\!E}$ s to Output in Low-Z	t <sub>CLZ</sub>	—	10	—	nS
$\overline{O\!E}$ to Output in Low-Z	t <sub>OLZ</sub>	—	5	—	nS
Output Hold from Address Change	t <sub>OH</sub>	—	10	—	nS
$\overline{C\!E}$ s to Output in High-Z	t <sub>CHZ</sub>	—	—	35	nS
$\overline{O\!E}$ to Output in High-Z	t <sub>OHZ</sub>	—	—	35	nS

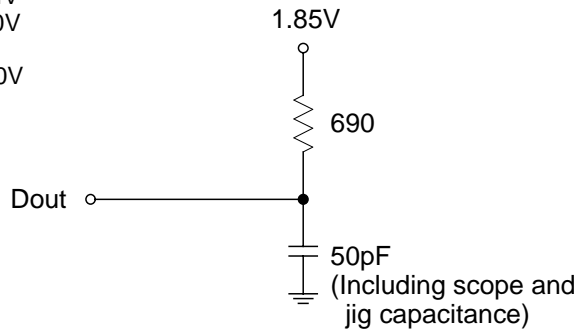
**SRAM Write Cycle (1)**

(V<sub>CC</sub>=3.0V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Write Cycle Time	t <sub>WC</sub>	—	100	—	nS
Address Setup Time	t <sub>AS</sub>	—	0	—	nS
Write Pulse Width	t <sub>WP</sub>	—	75	—	nS
Write Recovery Time	t <sub>WR</sub>	—	0	—	nS
Data Setup Time	t <sub>DS</sub>	—	40	—	nS
Data Hold Time	t <sub>DH</sub>	—	0	—	nS
$\overline{W\!E}$ to Output in High-Z	t <sub>WHZ</sub>	—	—	35	nS
$\overline{C\!E}$ s to End of Write	t <sub>CW</sub>	—	90	—	nS
Address Valid to End of Write	t <sub>AW</sub>	—	90	—	nS
Output Active from End of Write	t <sub>WLZ</sub>	—	5	—	nS

Test Condition

- Input Pulse Levels ----- 0.4V/2.4V
- Input Timing Reference Levels ----- 0.8V/2.0V
- Output Load ----- 50pF
- Output Timing Reference Levels ----- 0.8V/2.0V
- Input Rise and Fall Time ----- 5nS



**SRAM Read Cycle (2)**

(V<sub>CC</sub>=3.3V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t <sub>RC</sub>	—	80	—	nS
Address Access Time	t <sub>AA</sub>	—	—	80	nS
$\overline{C\!E}$ s Access Time	t <sub>CO</sub>	—	—	80	nS
$\overline{O\!E}$ Access Time	t <sub>OE</sub>	—	—	40	nS
$\overline{C\!E}$ s to Output in Low-Z	t <sub>CLZ</sub>	—	10	—	nS
$\overline{O\!E}$ to Output in Low-Z	t <sub>OLZ</sub>	—	5	—	nS
Output Hold from Address Change	t <sub>OH</sub>	—	10	—	nS
$\overline{C\!E}$ s to Output in High-Z	t <sub>CHZ</sub>	—	—	30	nS
$\overline{O\!E}$ to Output in High-Z	t <sub>OHZ</sub>	—	—	30	nS

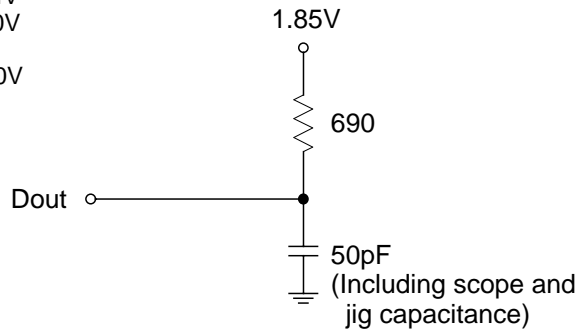
**SRAM Write Cycle (2)**

(V<sub>CC</sub>=3.3V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Write Cycle Time	t <sub>WC</sub>	—	80	—	nS
Address Setup Time	t <sub>AS</sub>	—	0	—	nS
Write Pulse Width	t <sub>WP</sub>	—	60	—	nS
Write Recovery Time	t <sub>WR</sub>	—	0	—	nS
Data Setup Time	t <sub>DS</sub>	—	35	—	nS
Data Hold Time	t <sub>DH</sub>	—	0	—	nS
$\overline{W\!E}$ to Output in High-Z	t <sub>WHZ</sub>	—	—	30	nS
$\overline{C\!E}$ s to End of Write	t <sub>CW</sub>	—	70	—	nS
Address Valid to End of Write	t <sub>AW</sub>	—	70	—	nS
Output Active from End of Write	t <sub>WLZ</sub>	—	5	—	nS

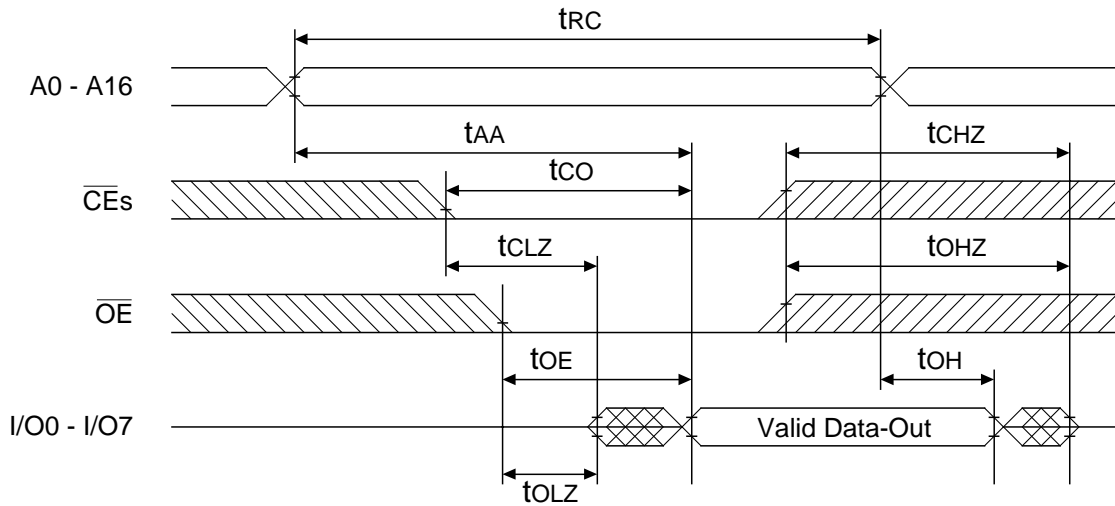
Test Condition

- Input Pulse Levels ----- 0.4V/2.4V
- Input Timing Reference Levels ----- 0.8V/2.0V
- Output Load ----- 50pF
- Output Timing Reference Levels ----- 0.8V/2.0V
- Input Rise and Fall Time ----- 5nS



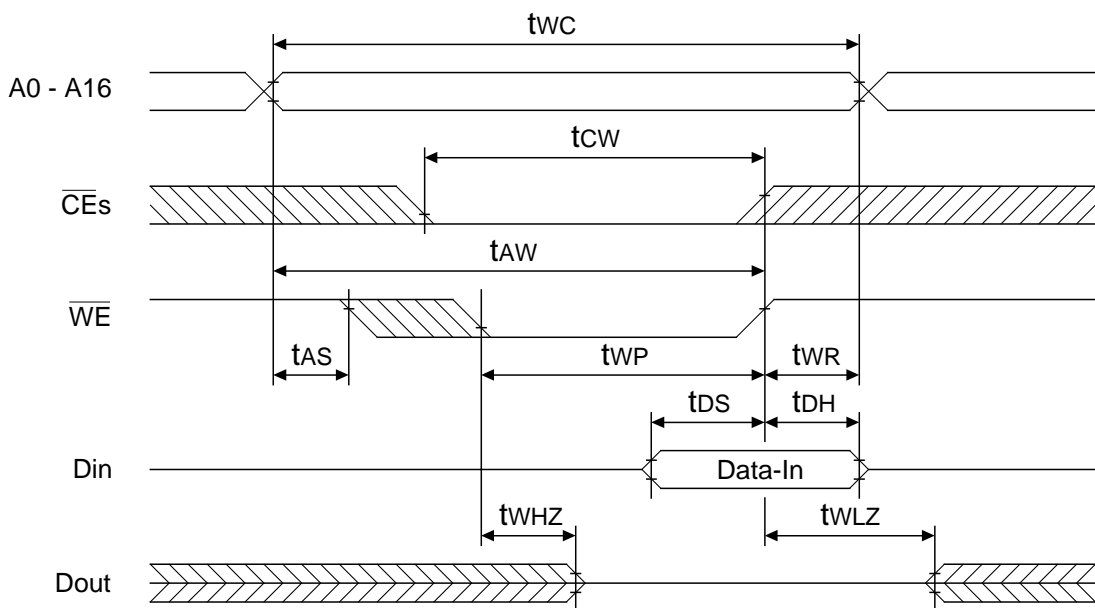
SRAM Timing Diagrams

SRAM Read Cycle



- Notes : 1. A read cycle of SRAM occurs during the overlap of  $\overline{CEo}="H"$ ,  $\overline{CEs}="L"$ ,  $\overline{OE}="L"$  and  $\overline{WE}="H"$ .  
 2.  $t_{OHZ}$ ,  $t_{CHZ}$  are specified by the time when DATA is floating, not defined by the output level.

SRAM Write Cycle

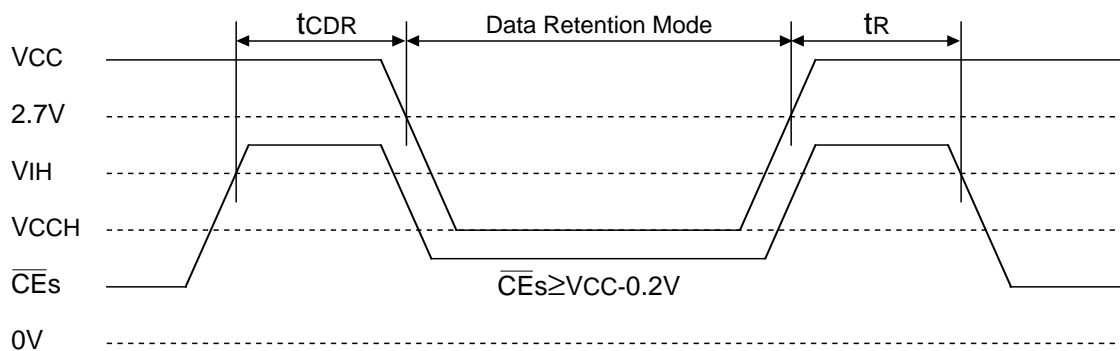


- Notes :
1. A write cycle of SRAM occurs during the overlap of  $\overline{CE}_0="H"$  ,  $\overline{CE}_s="L"$  and  $\overline{WE}="L"$ .
  2.  $\overline{OE}$  may be either of "H" or "L" in the write cycle of SRAM.
  3.  $t_{AS}$  is specified from  $\overline{CE}_s="L"$  or  $\overline{WE}="L"$  , whichever occurs last.
  4.  $t_{WP}$  is an overlap time of  $\overline{CE}_s="L"$  and  $\overline{WE}="L"$ .
  5.  $t_{WR}$  ,  $t_{DS}$  ,  $t_{DH}$  are specified from  $\overline{CE}_s="H"$  or  $\overline{WE}="H"$  , whichever occurs first.
  6.  $t_{WHZ}$  is specified by the time when DATA output is floating , not defined by the output level.
  7. When I/O pins are in the output mode , don't apply the inverted input signal to the output pins.

**SRAM Data Retention Characteristics**

( $T_a=-20$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Retention Power Supply Voltage	V <sub>CCH</sub>	$\overline{CE}_0 \geq V_{CC}-0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ $V_{IN}=0$ to $V_{CC}$	1.5	—	—	V
Data Retention Power Supply Current	I <sub>CCH</sub>	$V_{CC}=1.5V$ $\overline{CE}_0 \geq V_{CC}-0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ $V_{IN}=0$ to $V_{CC}$	—	—	3	$\mu\text{A}$
Chip Deselect to Data Retention Time	t <sub>CDR</sub>	—	0	—	—	nS
Operation Recovery Time	t <sub>R</sub>	—	5	—	—	mS



**OTP AC Characteristics (1)****OTP Read Cycle (1)**(V<sub>CC</sub>=3.0V±0.3V, T<sub>a</sub>=-20 to 70°C)

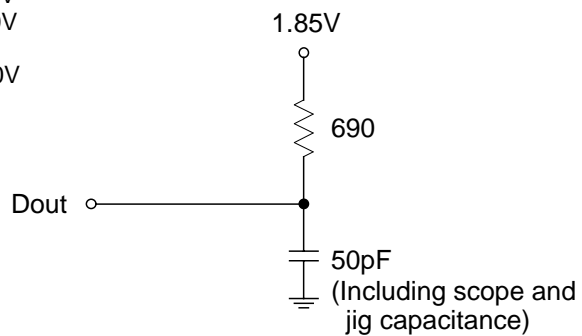
Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t <sub>RC</sub>	—	100	—	nS
Address Access Time	t <sub>AA</sub>	$\overline{CE}_0 = \overline{OE} = V_{IL}$	—	100	nS
$\overline{CE}_0$ Access Time	t <sub>CO</sub>	$\overline{OE} = V_{IL}$	—	100	nS
$\overline{OE}$ Access Time	t <sub>OE</sub>	$\overline{CE}_0 = V_{IL}$	—	50	nS
$\overline{CE}_0$ to Output in High-Z	t <sub>CHZ</sub>	$\overline{OE} = V_{IL}$	0	40	nS
$\overline{OE}$ to Output in High-Z	t <sub>OHZ</sub>	$\overline{CE}_0 = V_{IL}$	0	35	nS
Output Hold from Address Change	t <sub>OH</sub>	$\overline{CE}_0 = \overline{OE} = V_{IL}$	0	—	nS

**OTP Read Cycle (2)**(V<sub>CC</sub>=3.3V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t <sub>RC</sub>	—	80	—	nS
Address Access Time	t <sub>AA</sub>	$\overline{CE}_0 = \overline{OE} = V_{IL}$	—	80	nS
$\overline{CE}_0$ Access Time	t <sub>CO</sub>	$\overline{OE} = V_{IL}$	—	80	nS
$\overline{OE}$ Access Time	t <sub>OE</sub>	$\overline{CE}_0 = V_{IL}$	—	50	nS
$\overline{CE}_0$ to Output in High-Z	t <sub>CHZ</sub>	$\overline{OE} = V_{IL}$	0	40	nS
$\overline{OE}$ to Output in High-Z	t <sub>OHZ</sub>	$\overline{CE}_0 = V_{IL}$	0	35	nS
Output Hold from Address Change	t <sub>OH</sub>	$\overline{CE}_0 = \overline{OE} = V_{IL}$	0	—	nS

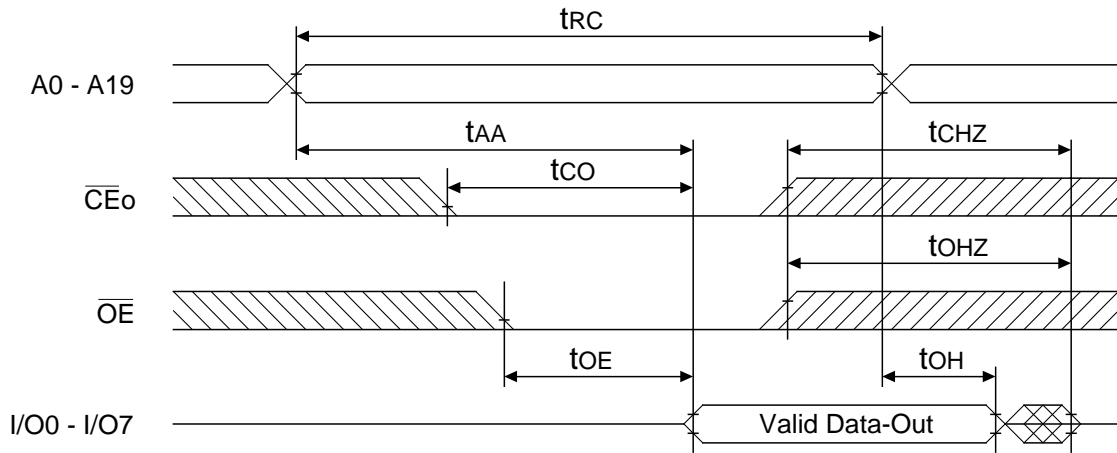
## Test Condition

Input Pulse Levels ----- 0.4V/2.4V  
 Input Timing Reference Levels ----- 0.8V/2.0V  
 Output Load ----- 50pF  
 Output Timing Reference Levels ----- 0.8V/2.0V  
 Input Rise and Fall Time ----- 5nS



**OTP Timing Diagrams**

**OTP Read Cycle**



- Notes : 1. A read cycle of OTP occurs during the overlap of  $\overline{CEo}$ ="L",  $\overline{CEs}$ ="H" and  $\overline{OE}$ ="L".  
 2.  $t_{OHZ}$  ,  $t_{CHZ}$  are specified by the time when DATA is floating , not defined by the output level.

**OTP DC Characteristics**

**OTP Programming Operation**

( $T_a=25^\circ\text{C}\pm 5^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$I_{LI}$	$V_I=V_{CC}+0.5V$	—	—	10	$\mu\text{A}$
Program Power Supply Current	$I_{PP2}$	$\overline{CEo}=V_{IL}$	—	—	50	mA
Power Supply Current	$I_{CC}$	—	—	—	50	mA
Input High Voltage	$V_{IH}$	—	3.0	—	$V_{CC}+0.5$	V
Input Low Voltage	$V_{IL}$	—	-0.5	—	0.8	V
Output High Voltage	$V_{OH}$	$I_{OH}=-500\mu\text{A}$	2.4	—	—	V
Output Low Voltage	$V_{OL}$	$I_{OL}=2.1\text{mA}$	—	—	0.45	V
Program Voltage	$V_{PP}$	—	9.5	9.75	10.0	V
VCC Voltage	$V_{CC}$	—	3.9	4.0	4.1	V

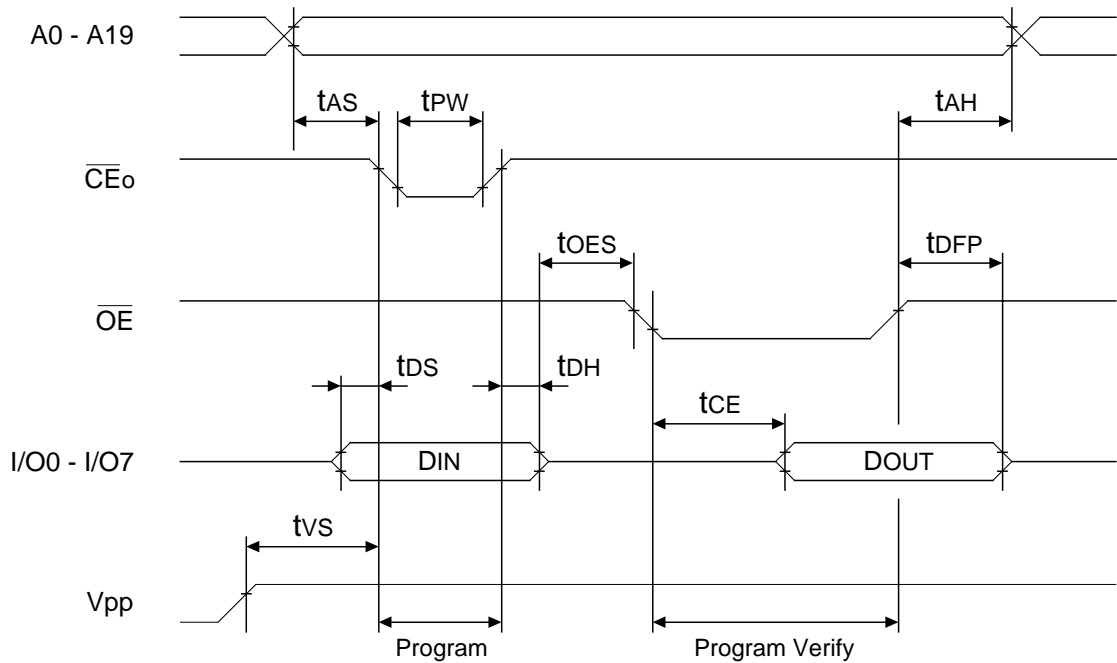
## OTP AC Characteristics (2)

### OTP Programming Operation

( $V_{CC}=4.0V\pm 0.1V$ ,  $V_{PP}=9.75V\pm 0.25V$ ,  $T_a=25^{\circ}C\pm 5^{\circ}C$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address Setup Time	tAS	—	2	—	—	$\mu S$
$\overline{OE}$ Setup Time	tOES	—	2	—	—	$\mu S$
Data Setup Time	tDS	—	2	—	—	$\mu S$
Address Hold Time	tAH	—	0	—	—	$\mu S$
Data Hold Time	tDH	—	2	—	—	$\mu S$
OE to Output in High-Z	tDFP	—	0	—	130	nS
VPP Power Setup Time	tVS	—	2	—	—	$\mu S$
Program Pulse Width	tPW	—	9	10	11	$\mu S$
Data Valid from $\overline{OE}$	tOE	—	—	—	150	nS

### OTP Programming Waveform



Note : When OTP is programming mode ,  $\overline{CE}_s$  should be "H" level.

### Pin Check Function

Pin Check Function is to check contact between each device-pin and each socket-lead with EPROM programmer.

Setting up address as the following condition call the preprogrammed codes on device outputs.

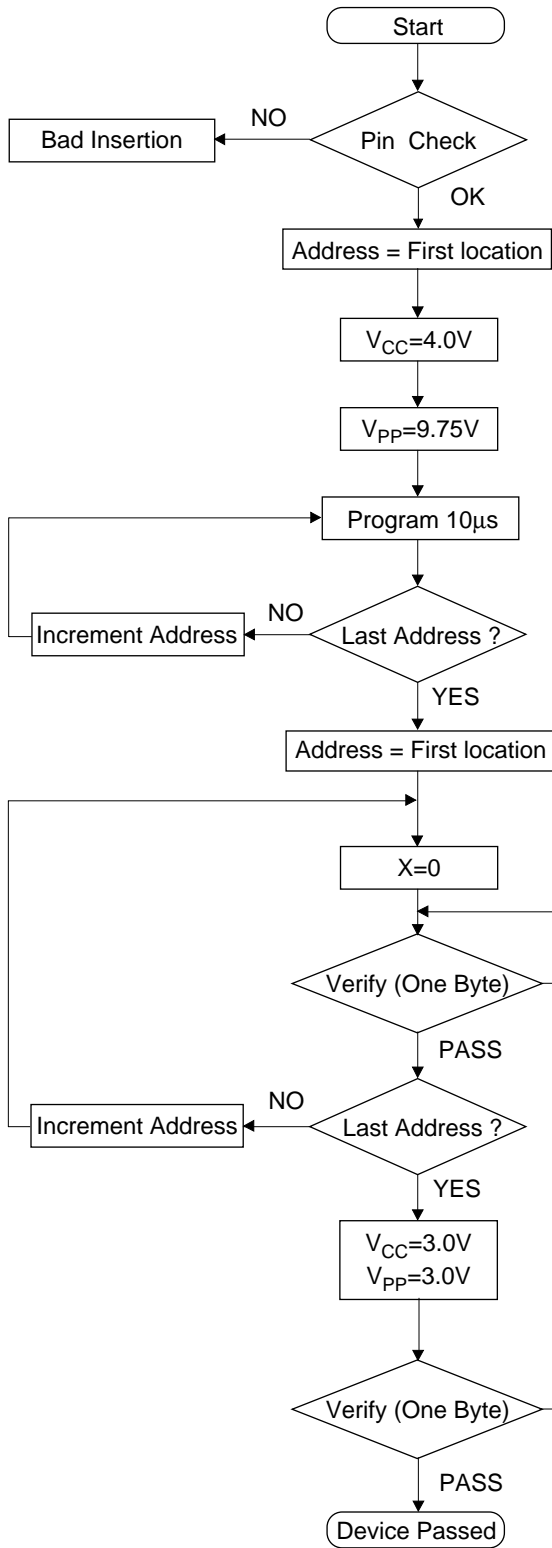
$$(V_{CC}=3.3V\pm 0.3V, \overline{CE}_O=V_{IL}, T_a=25^{\circ}C\pm 5^{\circ}C)$$

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A17	A18	A19	DATA
0	1	0	1	0	1	0	1	0	VH*	0	1	0	1	0	1	0	0	1	00
1	0	1	0	1	0	1	0	1	VH*	1	0	1	0	1	0	1	1	0	FF

\* :VH=8V

OTP Programming / Verify Flow Chart

Programming



Verify

