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**MS52C182A****Preliminary**

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65,536-Word X 16-Bit or 131,072-Word X 8-Bit STATIC RAM +  
524,288-Word X 16-Bit or 1,048,576-Word X 8-Bit One Time PROM

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**DESCRIPTION**

The MS52C182A is a 65,536 -word by 16 -bit / 131,072-word by 8-bit electrically switchable 1Mb static RAM and 524,288-word by 16-bit / 1,048,576-word by 8-bit electrically switchable 8Mb One Time PROM featuring 2.7V to 3.6V power supply operation and direct LVTTTL input / output compatibility. Since the circuitry is completely static, external clocks are unnecessary, making this device very easy to use.

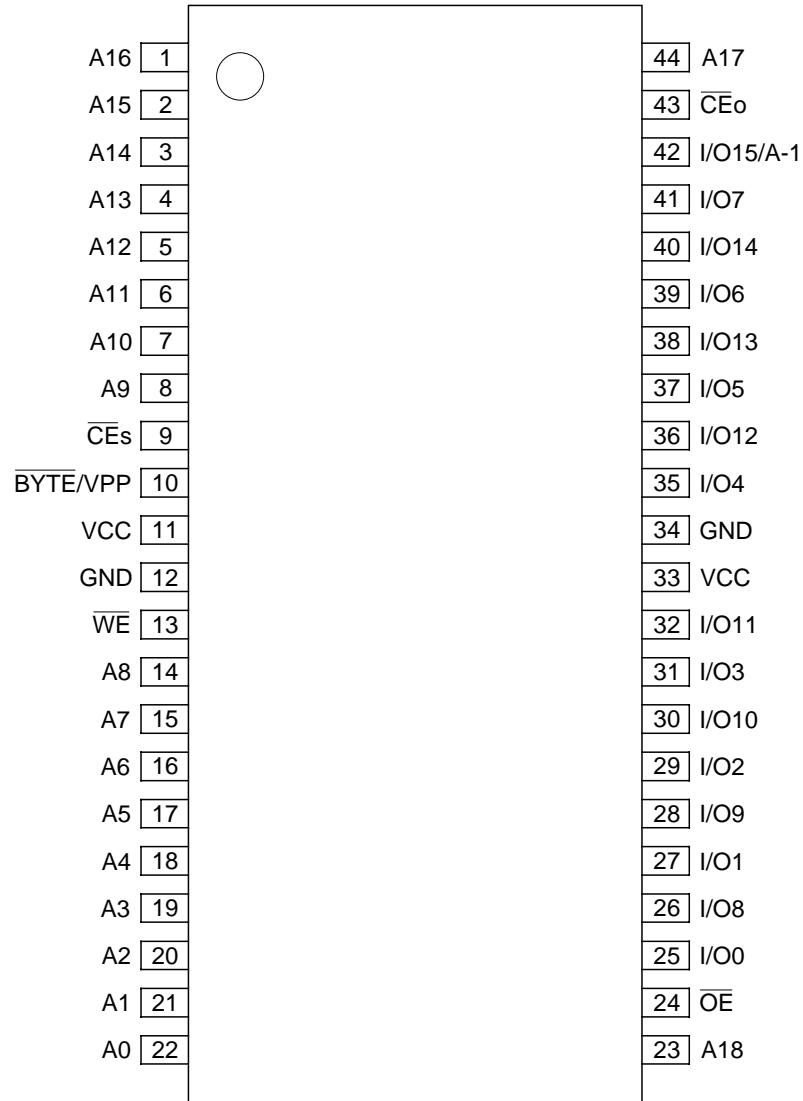
The MS52C182A is packaged in 44-pin plastic TSOP and 48-pin FBGA (9mmx10mm) ,suited for use in handy terminal and other application which required small space.

**FEATURES**

- 65,536-word x 16-bit / 131,072-word x 8-bit configuration SRAM and 524,288-word x 16-bit / 1,048,576-word x 8-bit configuration OTP
- Power supply voltage : 2.7 to 3.6V
- Fully static operation
- Operating temperature range : Ta= -20 to 70°C
- Access time : 100nS MAX (Vcc=2.7V)  
80nS MAX (Vcc=3.0V)
- Common address inputs and data inputs / outputs for SRAM and OTP
- Input / Output LVTTTL compatible
- 3-state output
- Data retention available at power supply voltage 1.5V for SRAM
- Package options :

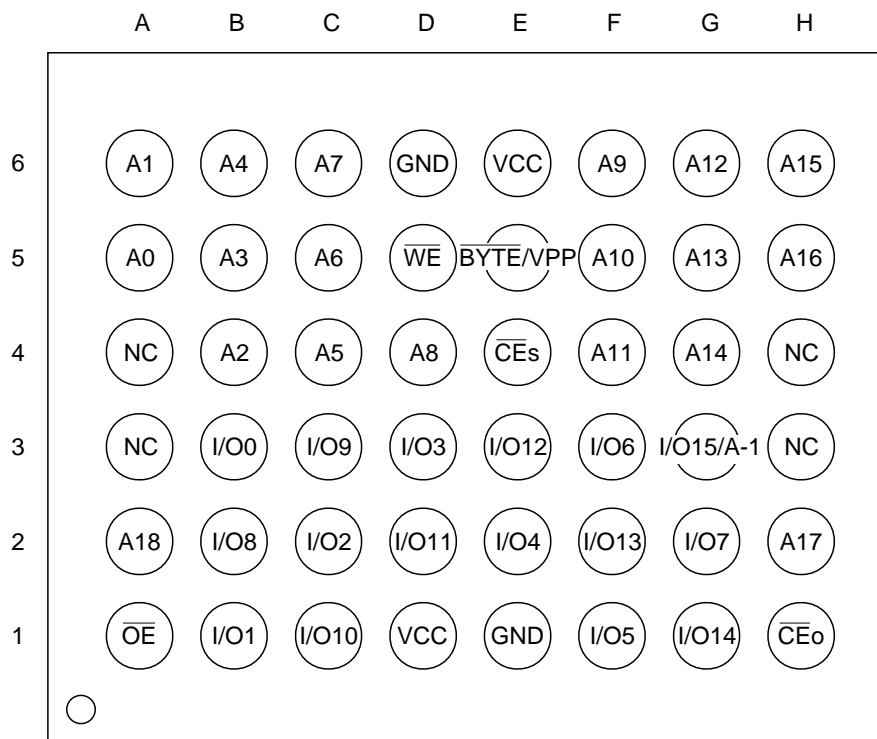
44-pin plastic TSOP (Type II)	(TSOP44-P-400-0.8)	(Product : MS52C182ATA)
48-pin plastic FBGA	(FBGA48-P-0910-0.8)	(Product : MS52C182ALA)

PIN CONFIGURATION (TOP VIEW)



44-pin TSOP (II)

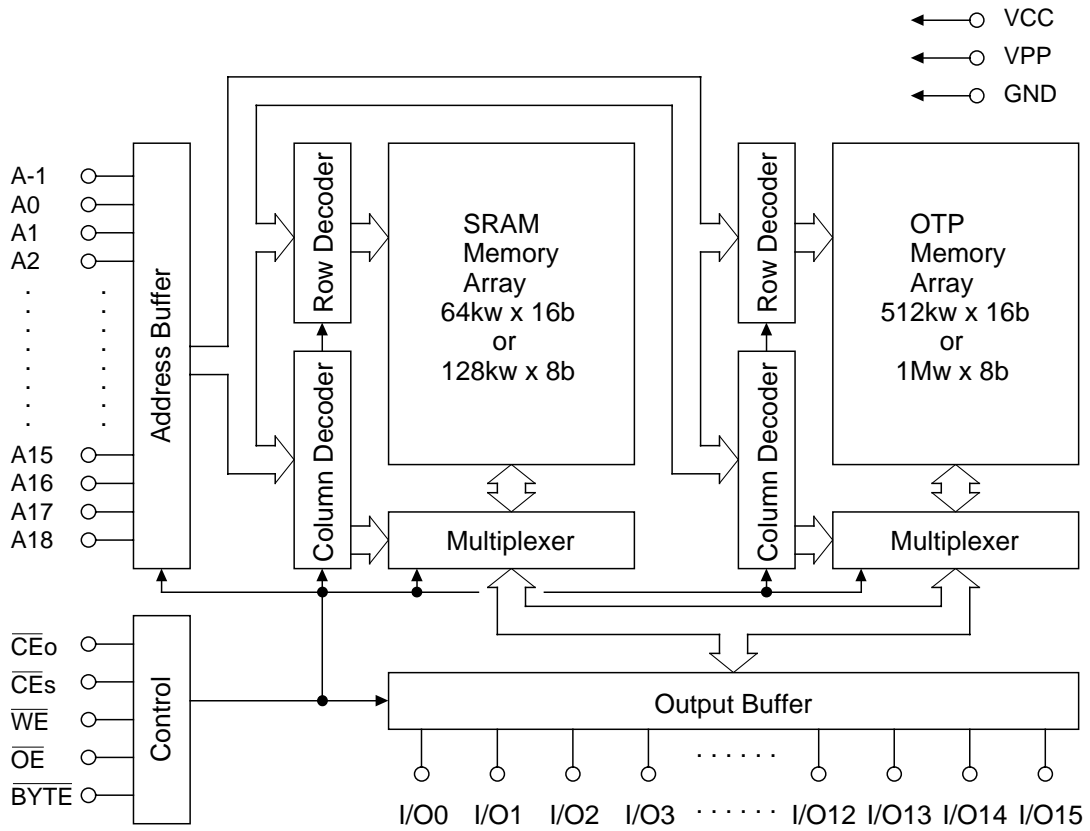
## PIN CONFIGURATION (TOP VIEW)



48-pin FBGA

Pin Name	Function
A -1 - A15	Common Address Inputs
A16 - A18	Address Inputs for OTP
$\overline{CEs}$	Chip Enable for SRAM
$\overline{CEo}$	Chip Enable for OTP
$\overline{WE}$	Write Enable for SRAM
$\overline{OE}$	Common Output Enable
I/O0 - I/O15	Common Data Inputs / Outputs
VCC	Common Power Supply
$\overline{BYTE/VPP}$	Common Mode Switch & Program Power Supply for OTP
GND	Common Ground
NC	No Connection

**BLOCK DIAGRAM**



**FUNCTION TABLE**

Operating Mode		$\overline{CE}_o$	$\overline{CE}_s$	$\overline{WE}$	$\overline{OE}$	BYTE / VPP	VCC	I/O0 - I/O7	I/O8 - I/O14	I/O15 / A-1
Standby		H	H	*	*	H	2.7V to 3.6V	High-Z	High-Z	High-Z
		H	H	*	*	L		High-Z	High-Z	*
SRAM Read	16-Bit	H	L	H	H	H		High-Z	High-Z	High-Z
		H	L	H	L	H		DOUT	DOUT	DOUT
	8-Bit	H	L	H	H	L		High-Z	High-Z	*
		H	L	H	L	L		DOUT	High-Z	L / H
SRAM Write	16-Bit	H	L	L	*	H		DIN	DIN	DIN
	8-Bit	H	L	L	*	L		DIN	High-Z	L / H
OTP Read	16-Bit	L	H	*	H	H		High-Z	High-Z	High-Z
		L	H	*	L	H		DOUT	DOUT	DOUT
	8-Bit	L	H	*	H	L	High-Z	High-Z	*	
		L	H	*	L	L	DOUT	High-Z	L / H	

Note : 1. \* = Don't Care ("H" or "L")  
 2. It is forbidden to apply  $\overline{CE}_o="L"$  and  $\overline{CE}_s="L"$  simultaneously.

## FUNCTION TABLE (Continued)

Operating Mode	$\overline{CE}_0$	$\overline{CE}_s$	$\overline{WE}$	$\overline{OE}$	$\overline{BYTE}/VPP$	VCC	I/O0 - I/O7	I/O8 - I/O14	I/O15 / A-1
OTP Program	L	H	*	H	9.75V	4.0V	DIN	DIN	DIN
OTP Program Inhibit	H	H	*	H			High-Z	High-Z	High-Z
OTP Program Verify	H	H	*	L			DOUT	DOUT	DOUT

Note : 1. \* = Don't Care ("H" or "L")

2. It is forbidden to apply  $\overline{CE}_0="L"$  and  $\overline{CE}_s="L"$  simultaneously.

## ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	VCC	Respect to GND	-0.5 to 5.0	V
	VPP		-0.5 to 11.5	V
Input Voltage	VI		-0.5* to Vcc+0.5	V
Output Voltage	VO		-0.5* to Vcc+0.5	V
Power Dissipation	PD	Ta=25°C	0.7	W
Operating Temperature	Topr	—	-20 to 70	°C
Storage Temperature	Tstg	—	-55 to 125	°C

\* -1.2VMin. for pulse width less than 30nS.

## Recommended Operating Conditions

(Ta= -20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	VCC	—	2.7	—	3.6	V
	VPP		-0.5	—	Vcc+0.5	V
	GND		0	0	0	V
SRAM Data Retention Voltage	VCCH	—	1.5	—	3.6	V
Input High Voltage	VIH	Vcc=2.7 to 3.6	2.2	—	Vcc+0.5	V
Input Low Voltage	VIL		-0.5*	—	0.4	V

\* -1.2VMin. for pulse width less than 30nS.

## DC Characteristics (1)

(V<sub>CC</sub>=3.0V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =0 to V <sub>CC</sub>	-1.0	—	1.0	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CE}_o=V_{IH}$ , $\overline{CE}_s=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>OUT</sub> =0 to V <sub>CC</sub>	-1.0	—	1.0	μA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-500μA	V <sub>CC</sub> -0.5	—	—	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	—	—	0.4	V
Standby Power Supply Current	I <sub>CCS</sub>	$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ V <sub>IN</sub> =0 to V <sub>CC</sub>	—	—	10	μA
	I <sub>CCS1</sub>	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	—	—	0.3	mA
Operating Power Supply Current	I <sub>CCA</sub> (SRAM)	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IL}$ $\overline{OE}=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> /V <sub>IL</sub> T <sub>CYC</sub> =100nS	—	—	35	mA
		$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \leq 0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V V <sub>IL</sub> ≤ 0.2V T <sub>CYC</sub> =1μS	—	—	10	mA
	I <sub>CCA</sub> * (OTP)	$\overline{CE}_o=V_{IL}$ $\overline{CE}_s=V_{IH}$ $\overline{OE}=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> /V <sub>IL</sub> T <sub>CYC</sub> =100nS	—	—	35	mA
		$\overline{CE}_o \leq 0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V V <sub>IL</sub> ≤ 0.2V T <sub>CYC</sub> =1μS	—	—	20	mA
V <sub>PP</sub> Power Supply Current	I <sub>PP</sub>	$\overline{BYTE}/V_{PP}=V_{CC}$	—	—	10	μA

\* Read Current

## DC Characteristics (2)

(V<sub>CC</sub>=3.3V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =0 to V <sub>CC</sub>	-1.0	—	1.0	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CE}_o=V_{IH}$ , $\overline{CE}_s=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>OUT</sub> =0 to V <sub>CC</sub>	-1.0	—	1.0	μA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-500μA	V <sub>CC</sub> -0.5	—	—	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	—	—	0.4	V
Standby Power Supply Current	I <sub>CCS</sub>	$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ V <sub>IN</sub> =0 to V <sub>CC</sub>	—	—	10	μA
	I <sub>CCS1</sub>	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	—	—	0.3	mA
Operating Power Supply Current	I <sub>CCA</sub> (SRAM)	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IL}$ $\overline{OE}=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> /V <sub>IL</sub> TCYC=80nS	—	—	40	mA
		$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \leq 0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V V <sub>IL</sub> ≤ 0.2V TCYC=1μS	—	—	15	mA
	I <sub>CCA*</sub> (OTP)	$\overline{CE}_o=V_{IL}$ $\overline{CE}_s=V_{IH}$ $\overline{OE}=V_{IH}$ V <sub>IN</sub> =V <sub>IH</sub> /V <sub>IL</sub> TCYC=80nS	—	—	40	mA
		$\overline{CE}_o \leq 0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V V <sub>IL</sub> ≤ 0.2V TCYC=1μS	—	—	25	mA
V <sub>PP</sub> Power Supply Current	I <sub>PP</sub>	$\overline{BYTE}/V_{PP}=V_{CC}$	—	—	10	μA

\* Read Current

**SRAM AC Characteristics**

**SRAM Read Cycle (1)**

(V<sub>CC</sub>=3.0V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t <sub>RC</sub>	—	100	—	nS
Address Access Time	t <sub>AA</sub>	—	—	100	nS
$\overline{C\!E}$ s Access Time	t <sub>CO</sub>	—	—	100	nS
$\overline{O\!E}$ Access Time	t <sub>OE</sub>	—	—	50	nS
$\overline{C\!E}$ s to Output in Low-Z	t <sub>CLZ</sub>	—	10	—	nS
$\overline{O\!E}$ to Output in Low-Z	t <sub>OLZ</sub>	—	5	—	nS
Output Hold from Address Change	t <sub>OH</sub>	—	10	—	nS
$\overline{C\!E}$ s to Output in High-Z	t <sub>CHZ</sub>	—	—	35	nS
$\overline{O\!E}$ to Output in High-Z	t <sub>OHZ</sub>	—	—	35	nS

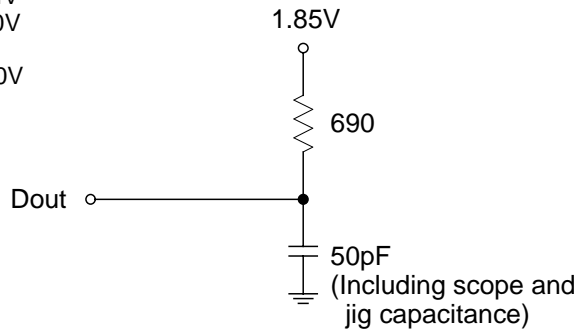
**SRAM Write Cycle (1)**

(V<sub>CC</sub>=3.0V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Write Cycle Time	t <sub>WC</sub>	—	100	—	nS
Address Setup Time	t <sub>AS</sub>	—	0	—	nS
Write Pulse Width	t <sub>WP</sub>	—	75	—	nS
Write Recovery Time	t <sub>WR</sub>	—	0	—	nS
Data Setup Time	t <sub>DS</sub>	—	40	—	nS
Data Hold Time	t <sub>DH</sub>	—	0	—	nS
$\overline{W\!E}$ to Output in High-Z	t <sub>WHZ</sub>	—	—	35	nS
$\overline{C\!E}$ s to End of Write	t <sub>CW</sub>	—	90	—	nS
Address Valid to End of Write	t <sub>AW</sub>	—	90	—	nS
Output Active from End of Write	t <sub>WLZ</sub>	—	5	—	nS

Test Condition

- Input Pulse Levels ----- 0.4V/2.4V
- Input Timing Reference Levels ----- 0.8V/2.0V
- Output Load ----- 50pF
- Output Timing Reference Levels ----- 0.8V/2.0V
- Input Rise and Fall Time ----- 5nS



**SRAM Read Cycle (2)**

(V<sub>CC</sub>=3.3V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t <sub>RC</sub>	—	80	—	nS
Address Access Time	t <sub>AA</sub>	—	—	80	nS
$\overline{C\!E}$ s Access Time	t <sub>CO</sub>	—	—	80	nS
$\overline{O\!E}$ Access Time	t <sub>OE</sub>	—	—	40	nS
$\overline{C\!E}$ s to Output in Low-Z	t <sub>CLZ</sub>	—	10	—	nS
$\overline{O\!E}$ to Output in Low-Z	t <sub>OLZ</sub>	—	5	—	nS
Output Hold from Address Change	t <sub>OH</sub>	—	10	—	nS
$\overline{C\!E}$ s to Output in High-Z	t <sub>CHZ</sub>	—	—	30	nS
$\overline{O\!E}$ to Output in High-Z	t <sub>OHZ</sub>	—	—	30	nS

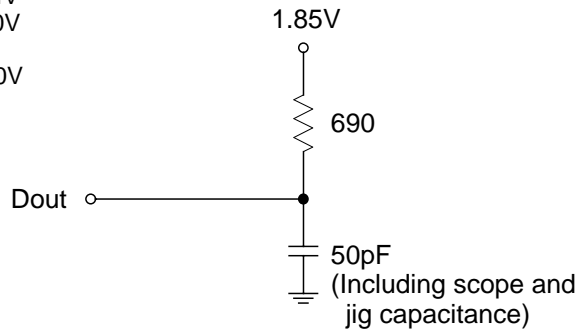
**SRAM Write Cycle (2)**

(V<sub>CC</sub>=3.3V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Write Cycle Time	t <sub>WC</sub>	—	80	—	nS
Address Setup Time	t <sub>AS</sub>	—	0	—	nS
Write Pulse Width	t <sub>WP</sub>	—	60	—	nS
Write Recovery Time	t <sub>WR</sub>	—	0	—	nS
Data Setup Time	t <sub>DS</sub>	—	35	—	nS
Data Hold Time	t <sub>DH</sub>	—	0	—	nS
$\overline{W\!E}$ to Output in High-Z	t <sub>WHZ</sub>	—	—	30	nS
$\overline{C\!E}$ s to End of Write	t <sub>CW</sub>	—	70	—	nS
Address Valid to End of Write	t <sub>AW</sub>	—	70	—	nS
Output Active from End of Write	t <sub>WLZ</sub>	—	5	—	nS

Test Condition

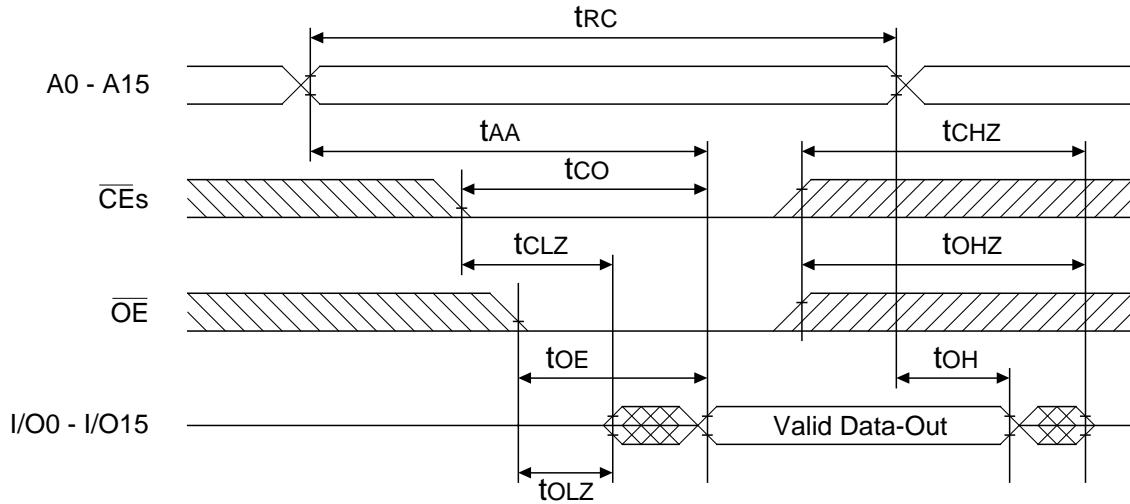
- Input Pulse Levels ----- 0.4V/2.4V
- Input Timing Reference Levels ----- 0.8V/2.0V
- Output Load ----- 50pF
- Output Timing Reference Levels ----- 0.8V/2.0V
- Input Rise and Fall Time ----- 5nS



SRAM Timing Diagrams

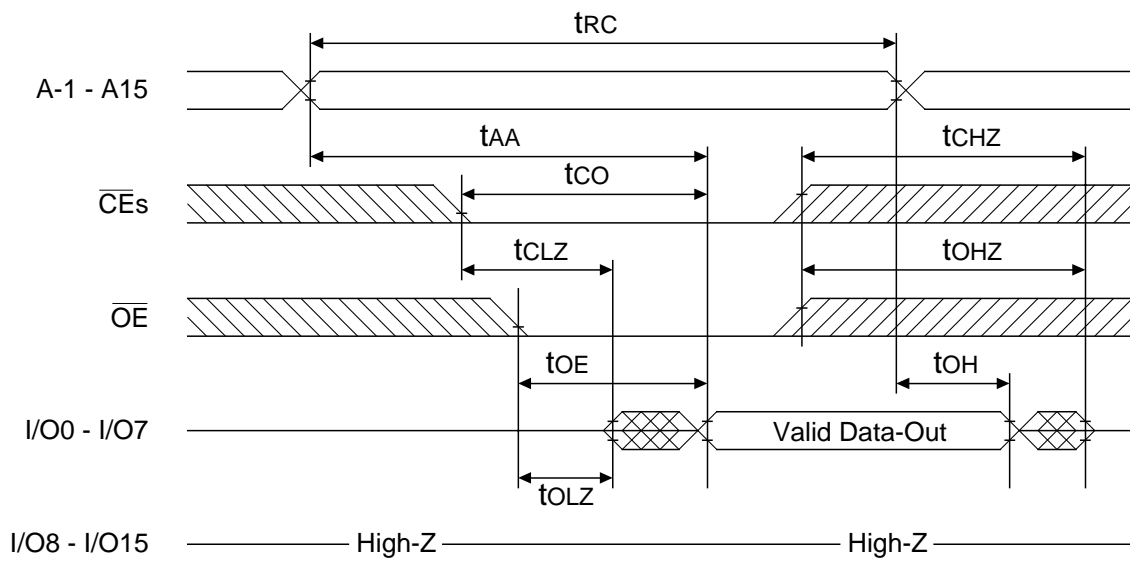
SRAM Read Cycle (1)

16-bit Read Mode (BYTE=VIH)



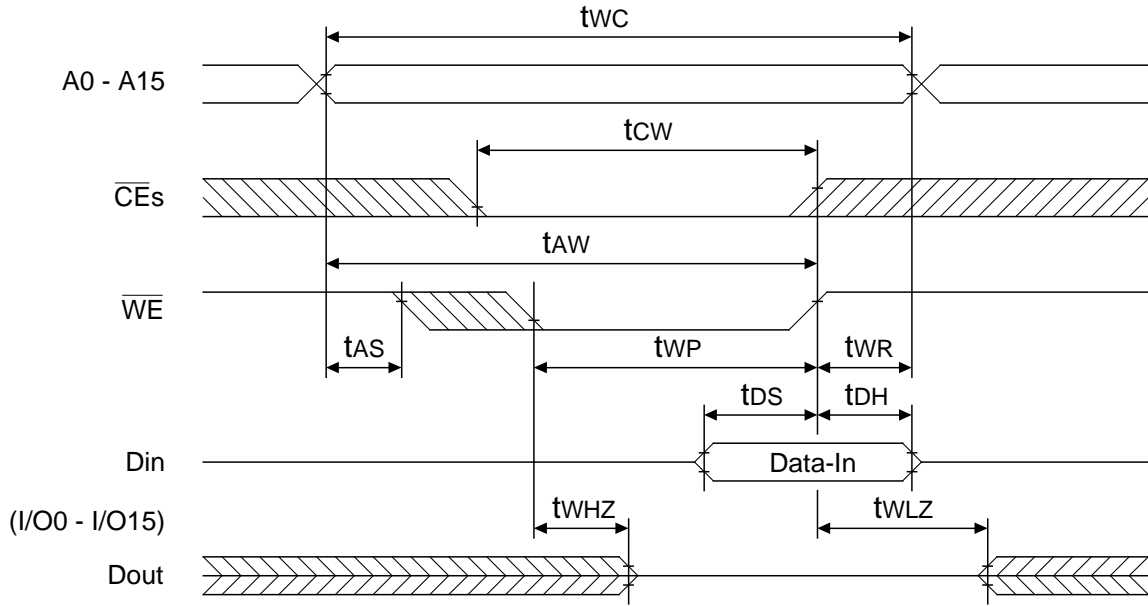
SRAM Read Cycle (2)

8-bit Read Mode (BYTE=VIL)

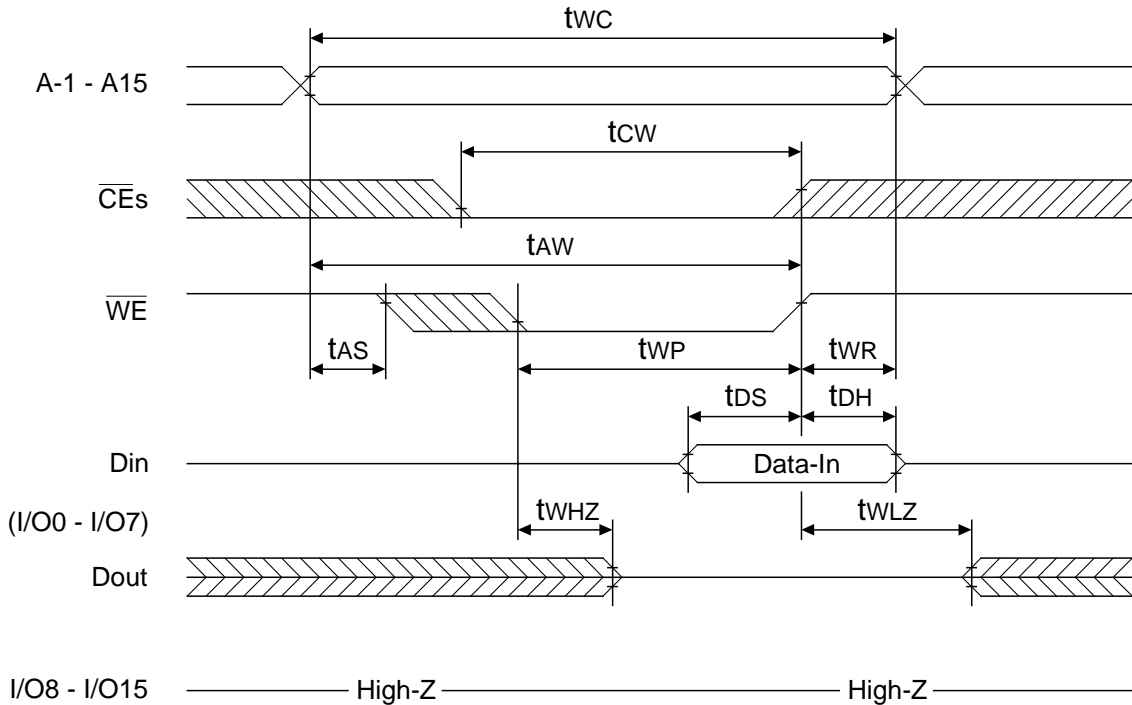


- Notes : 1. A read cycle of SRAM occurs during the overlap of  $\overline{CE}_o="H"$ ,  $\overline{CE}_s="L"$ ,  $\overline{OE}="L"$  and  $\overline{WE}="H"$ .  
 2.  $t_{OHZ}$  ,  $t_{CHZ}$  are specified by the time when DATA is floating , not defined by the output level.

**SRAM Write Cycle (1)**  
**16-bit Write Mode (BYTE=VIH)**



**SRAM Write Cycle (2)**  
**8-bit Write Mode (BYTE=VIL)**

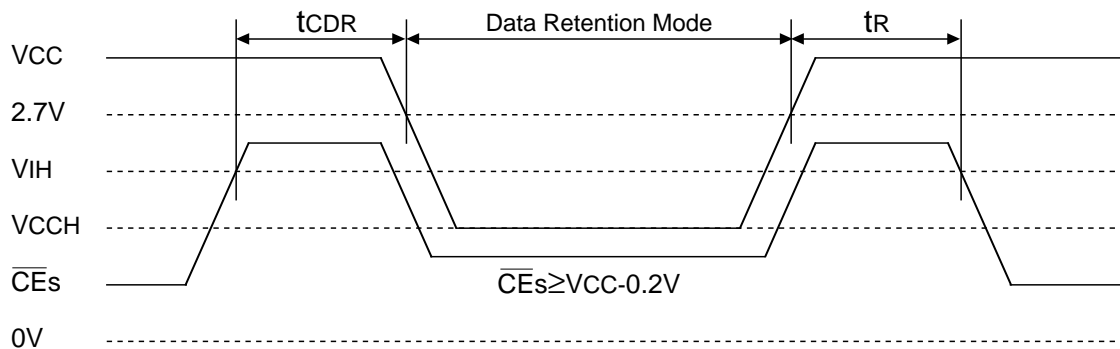


- Notes :
1. A write cycle of SRAM occurs during the overlap of  $\overline{CE}_0="H"$  ,  $\overline{CE}_s="L"$  and  $\overline{WE}="L"$ .
  2.  $\overline{OE}$  may be either of "H" or "L" in the write cycle of SRAM.
  3.  $t_{AS}$  is specified from  $\overline{CE}_s="L"$  or  $\overline{WE}="L"$  , whichever occurs last.
  4.  $t_{WP}$  is an overlap time of  $\overline{CE}_s="L"$  and  $\overline{WE}="L"$ .
  5.  $t_{WR}$  ,  $t_{DS}$  ,  $t_{DH}$  are specified from  $\overline{CE}_s="H"$  or  $\overline{WE}="H"$  , whichever occurs first.
  6.  $t_{WHZ}$  is specified by the time when DATA output is floating , not defined by the output level.
  7. When I/O pins are in the output mode , don't apply the inverted input signal to the output pins.

**SRAM Data Retention Characteristics**

( $T_a=-20$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Retention Power Supply Voltage	V <sub>CCH</sub>	$\overline{CE}_0 \geq V_{CC}-0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ $V_{IN}=0$ to $V_{CC}$	1.5	—	—	V
Data Retention Power Supply Current	I <sub>CCH</sub>	$V_{CC}=1.5V$ $\overline{CE}_0 \geq V_{CC}-0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ $V_{IN}=0$ to $V_{CC}$	—	—	3	$\mu\text{A}$
Chip Deselect to Data Retention Time	t <sub>CDR</sub>	—	0	—	—	nS
Operation Recovery Time	t <sub>R</sub>	—	5	—	—	mS



**OTP AC Characteristics (1)****OTP Read Cycle (1)**(V<sub>CC</sub>=3.0V±0.3V, T<sub>a</sub>=-20 to 70°C)

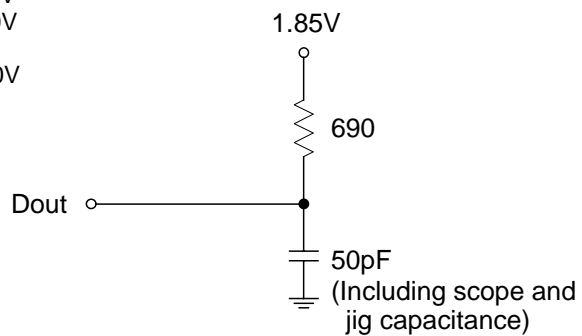
Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t <sub>RC</sub>	—	100	—	nS
Address Access Time	t <sub>AA</sub>	$\overline{CE}_0 = \overline{OE} = V_{IL}$	—	100	nS
$\overline{CE}_0$ Access Time	t <sub>CO</sub>	$\overline{OE} = V_{IL}$	—	100	nS
$\overline{OE}$ Access Time	t <sub>OE</sub>	$\overline{CE}_0 = V_{IL}$	—	50	nS
$\overline{CE}_0$ to Output in High-Z	t <sub>CHZ</sub>	$\overline{OE} = V_{IL}$	0	40	nS
$\overline{OE}$ to Output in High-Z	t <sub>OHZ</sub>	$\overline{CE}_0 = V_{IL}$	0	35	nS
Output Hold from Address Change	t <sub>OH</sub>	$\overline{CE}_0 = \overline{OE} = V_{IL}$	0	—	nS

**OTP Read Cycle (2)**(V<sub>CC</sub>=3.3V±0.3V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t <sub>RC</sub>	—	80	—	nS
Address Access Time	t <sub>AA</sub>	$\overline{CE}_0 = \overline{OE} = V_{IL}$	—	80	nS
$\overline{CE}_0$ Access Time	t <sub>CO</sub>	$\overline{OE} = V_{IL}$	—	80	nS
$\overline{OE}$ Access Time	t <sub>OE</sub>	$\overline{CE}_0 = V_{IL}$	—	50	nS
$\overline{CE}_0$ to Output in High-Z	t <sub>CHZ</sub>	$\overline{OE} = V_{IL}$	0	40	nS
$\overline{OE}$ to Output in High-Z	t <sub>OHZ</sub>	$\overline{CE}_0 = V_{IL}$	0	35	nS
Output Hold from Address Change	t <sub>OH</sub>	$\overline{CE}_0 = \overline{OE} = V_{IL}$	0	—	nS

## Test Condition

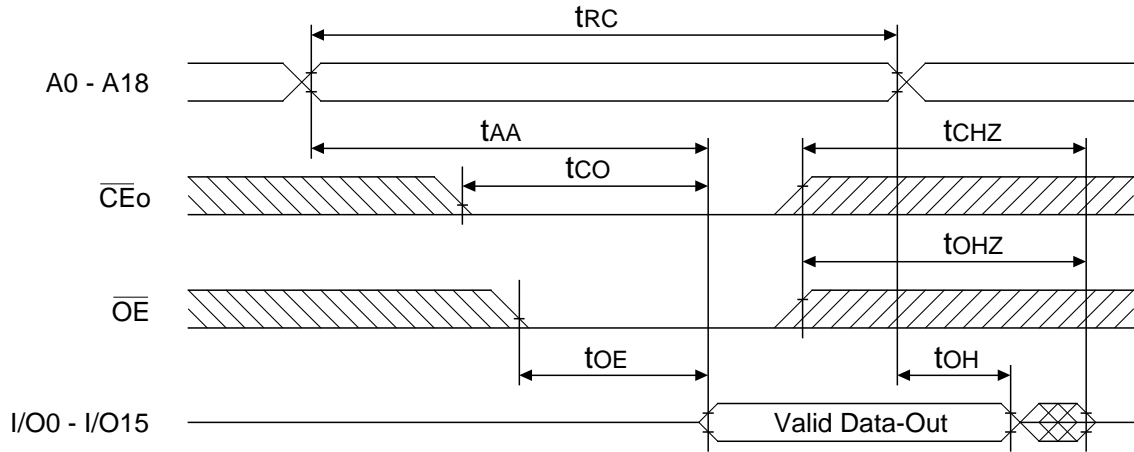
Input Pulse Levels ----- 0.4V/2.4V  
 Input Timing Reference Levels ----- 0.8V/2.0V  
 Output Load ----- 50pF  
 Output Timing Reference Levels ----- 0.8V/2.0V  
 Input Rise and Fall Time ----- 5nS



OTP Timing Diagrams

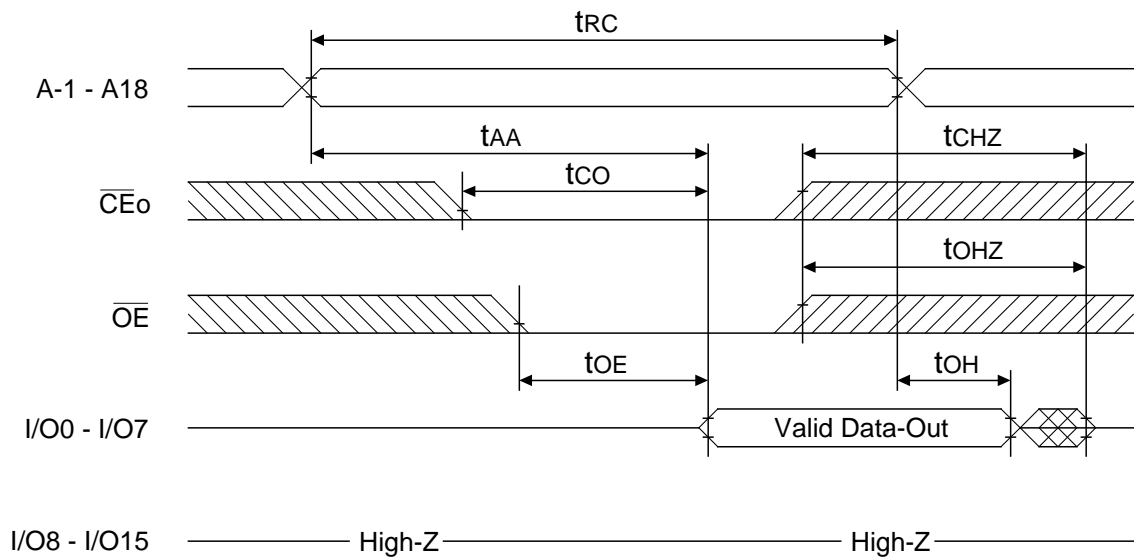
OTP Read Cycle (1)

16-bit Read Mode ( $\overline{\text{BYTE}}=\text{VIH}$ )



OTP Read Cycle (2)

8-bit Read Mode ( $\overline{\text{BYTE}}=\text{VIL}$ )



- Notes : 1. A read cycle of OTP occurs during the overlap of  $\overline{\text{CE}}_0=\text{"L"}$ ,  $\overline{\text{CE}}_s=\text{"H"}$  and  $\overline{\text{OE}}=\text{"L"}$ .  
 2.  $t_{OHZ}$  ,  $t_{CHZ}$  are specified by the time when DATA is floating , not defined by the output level.

**OTP DC Characteristics****OTP Programming Operation**

(Ta=25°C±5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	ILI	VI=VCC+0.5V	—	—	10	μA
Program Power Supply Current	I <sub>PP2</sub>	$\overline{CE}_0=V_{IL}$	—	—	50	mA
Power Supply Current	I <sub>CC</sub>	—	—	—	50	mA
Input High Voltage	V <sub>IH</sub>	—	3.0	—	VCC+0.5	V
Input Low Voltage	V <sub>IH</sub>	—	-0.5	—	0.8	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-500μA	2.4	—	—	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	—	—	0.45	V
Program Voltage	V <sub>PP</sub>	—	9.5	9.75	10.0	V
VCC Voltage	V <sub>CC</sub>	—	3.9	4.0	4.1	V

**OTP AC Characteristics (2)****OTP Programming Operation**(V<sub>CC</sub>=4.0V±0.1V, V<sub>PP</sub>=9.75V±0.25V, Ta=25°C±5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address Setup Time	t <sub>AS</sub>	—	2	—	—	μS
$\overline{OE}$ Setup Time	t <sub>OES</sub>	—	2	—	—	μS
Data Setup Time	t <sub>DS</sub>	—	2	—	—	μS
Address Hold Time	t <sub>AH</sub>	—	0	—	—	μS
Data Hold Time	t <sub>DH</sub>	—	2	—	—	μS
$\overline{OE}$ to Output in High-Z	t <sub>DFP</sub>	—	0	—	130	nS
V <sub>PP</sub> Power Setup Time	t <sub>VS</sub>	—	2	—	—	μS
Program Pulse Width	t <sub>PW</sub>	—	9	10	11	μS
Data Valid from $\overline{OE}$	t <sub>OE</sub>	—	—	—	150	nS

**Pin Check Function**

Pin Check Function is to check contact between each device-pin and each socket-lead with EPROM programmer.

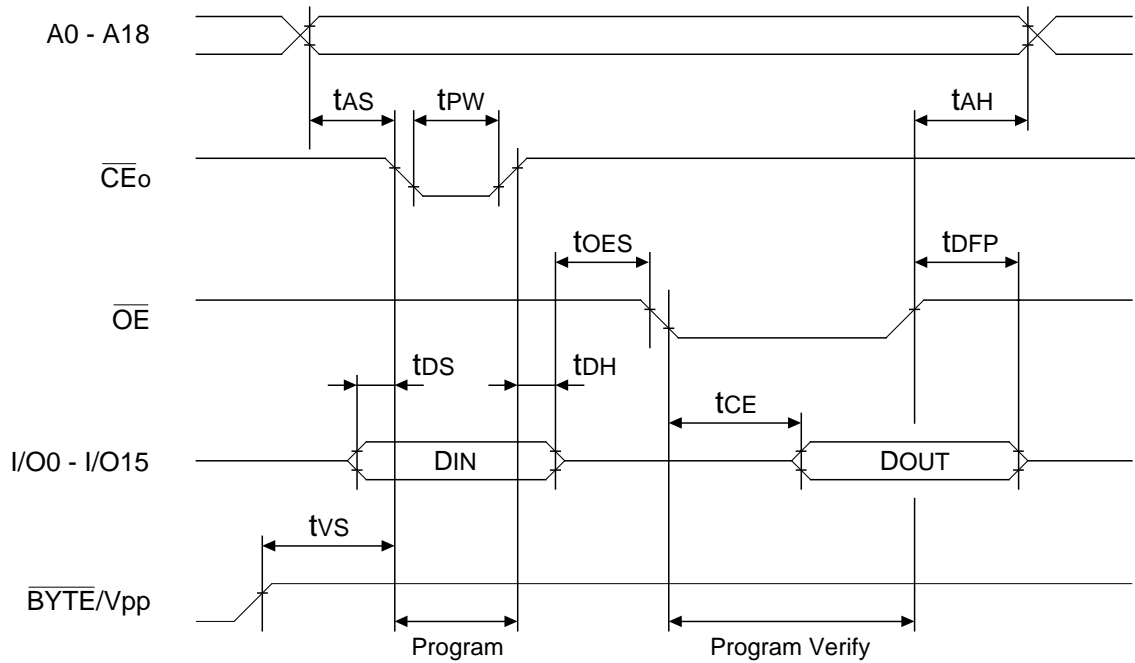
Setting up address as the following condition call the preprogrammed codes on device outputs.

(V<sub>CC</sub>=3.3V±0.3V,  $\overline{CE}_0=V_{IL}$ ,  $\overline{BYTE}/V_{pp}=V_{IH}$ , Ta=25°C±5°C)

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	DATA
0	1	0	1	0	1	0	1	0	VH*	0	1	0	1	0	1	0	0	1	FF00
1	0	1	0	1	0	1	0	1	VH*	1	0	1	0	1	0	1	1	0	00FF

\*:VH=8V

**OTP Programming Waveform**



Note : When OTP is programming mode ,  $\overline{CE}_o$  should be "H" level.

**Capacitance**

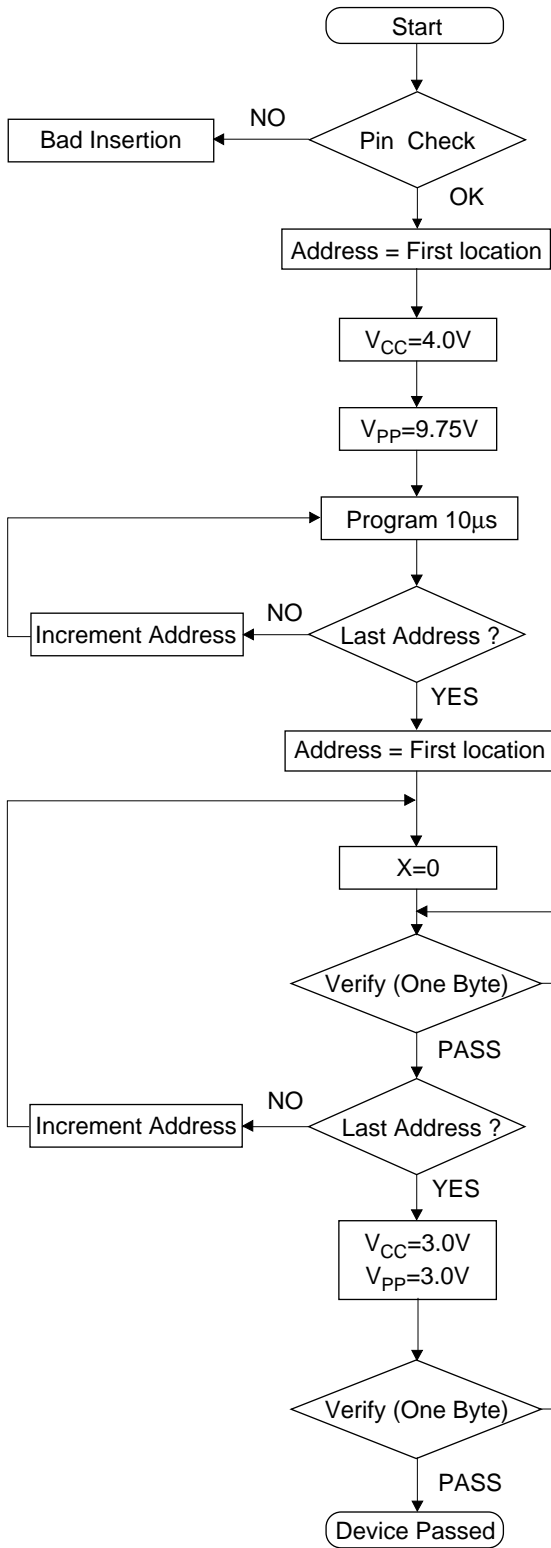
(Vcc=3.3V , Ta=25°C , f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Capacitance	CIN1	V I=0V	—	—	10	pF
BYTE/VPP Capacitance	CIN2		—	—	60	pF
Input/Output Capacitance	CI/O	VO=0V	—	—	10	pF

Note : This parameter is periodically sampled and not 100% tested.

OTP Programming / Verify Flow Chart

Programming



Verify

