

# OKI Semiconductor

FEDR27V3252J-01-02

Issue Date: Jul. 9, 2004

## MR27V3252J

**2M-Word × 16-Bit or 4M-Word × 8-Bit Page Mode OTP**

### GENERAL DESCRIPTION

The MR27V3252J is a 32 Mbit electrically One Time Programmable Read-Only Memory with page mode. Its configuration can be electrically switched between 2,097,152-word × 16-bit and 4,194,304-word × 8-bit by the state of the BYTE# pin. The MR27V3252J supports high speed asynchronous read operation using a single 3.3V power supply.

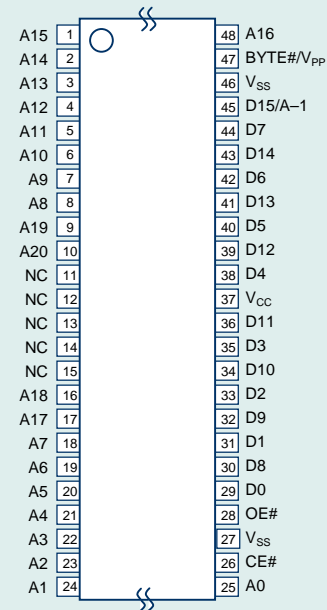
### FEATURES

- 2,097,152-word × 16-bit / 4,194,304-word × 8-bit electrically switchable configuration
- Page size of 8-word x 16-Bit or 16-word x 8-Bit
- 3.0 V to 3.6 V power supply
- Random Access time       70 ns MAX
- Page Access time         25 ns MAX
- Operating current         50 mA MAX
- Standby current          10 μA MAX
- Input/Output TTL compatible
- Three-state output

### PACKAGES

- MR27V3252JTN  
48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)

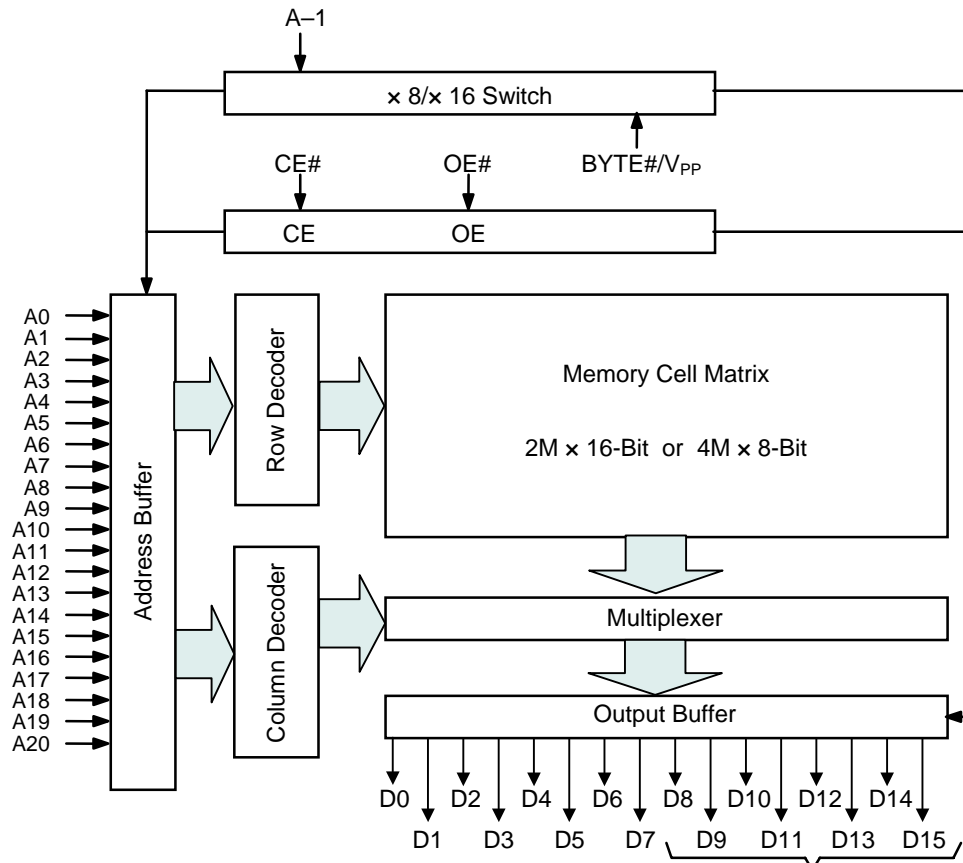
### PIN CONFIGURATION (TOP VIEW)



#### 48TSOP(Type-I)



## BLOCK DIAGRAM



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

## PIN DESCRIPTIONS

Pin name	Functions
D15 / A-1	Data output / Address input
A0 to A20	Address inputs
D0 to D14	Data outputs
CE#	Chip enable input
OE#	Output enable input
BYTE#/V <sub>PP</sub>	Mode switch/Program power supply voltage
V <sub>CC</sub>	Power supply voltage
V <sub>SS</sub>	Ground
NC	No connect

## FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V <sub>CC</sub>	D0 to D7	D8 to D14	D15/A-1
Read (16-Bit)	L	L	H	3.3 V	D <sub>OUT</sub>		
Read (8-Bit)	L	L	L		D <sub>OUT</sub>	Hi-Z	L/H
Output disable	L	H	H		Hi-Z		*
			L				
Standby	H	*	H		Hi-Z		*
			L				
Program	L	H	V <sub>PP</sub>	V <sub>CC</sub>	D <sub>IN</sub>		
Program inhibit	H	H			Hi-Z		
Program verify	H	L			D <sub>OUT</sub>		

\*: Don't Care (H or L)

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T <sub>a</sub>	—	0 to 70	°C
Storage temperature	T <sub>stg</sub>		-55 to 125	°C
Input voltage	V <sub>I</sub>	relative to V <sub>SS</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Output voltage	V <sub>O</sub>		-0.5 to V <sub>CC</sub> +0.5	V
Power supply voltage	V <sub>CC</sub>		-0.5 to 5	V
Program power supply voltage	V <sub>PP</sub>		-0.5 to 11.5	V
Power dissipation per package	P <sub>D</sub>		T <sub>a</sub> = 25°C	1.0
Output short circuit current	I <sub>OS</sub>	—	10	mA

## RECOMMENDED OPERATING CONDITIONS

(T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V <sub>CC</sub> power supply voltage	V <sub>CC</sub>	V <sub>CC</sub> = 3.0 to 3.6 V	3.0	—	3.6	V
V <sub>PP</sub> power supply voltage	V <sub>PP</sub>		-0.5	—	V <sub>CC</sub> +0.5	V
Input "H" level	V <sub>IH</sub>		2.2	—	V <sub>CC</sub> +0.5*	V
Input "L" level	V <sub>IL</sub>		-0.5**	—	0.6	V

Voltage is relative to V<sub>SS</sub>.

\* : V<sub>CC</sub>+1.5V(Max.) when pulse width of overshoot is less than 10ns.

\*\* : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

## PIN CAPACITANCE

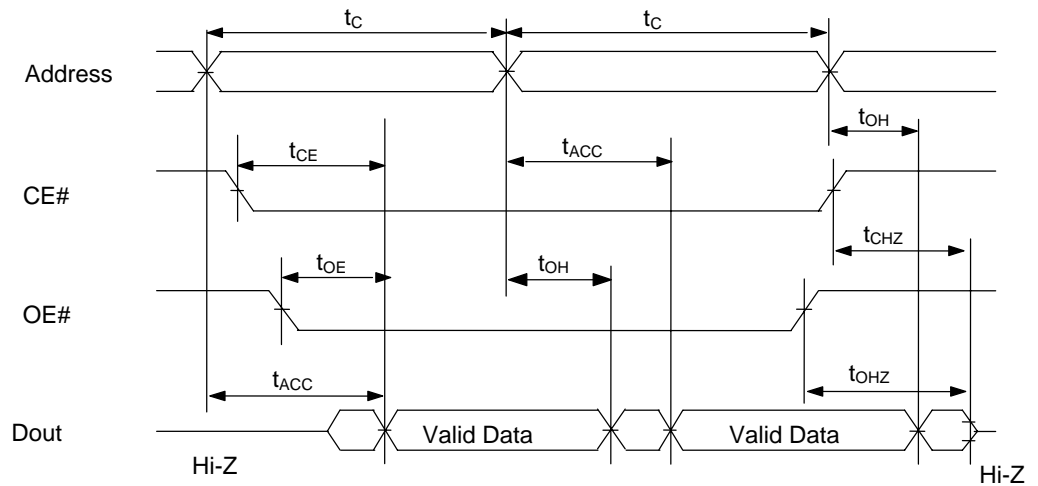
(V<sub>CC</sub> = 3.3 V, T<sub>a</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C <sub>IN1</sub>	V <sub>I</sub> = 0 V	—	—	8	pF
BYTE#/V <sub>PP</sub>	C <sub>IN2</sub>		—	—	200	
Output	C <sub>OUT</sub>	V <sub>O</sub> = 0 V	—	—	10	

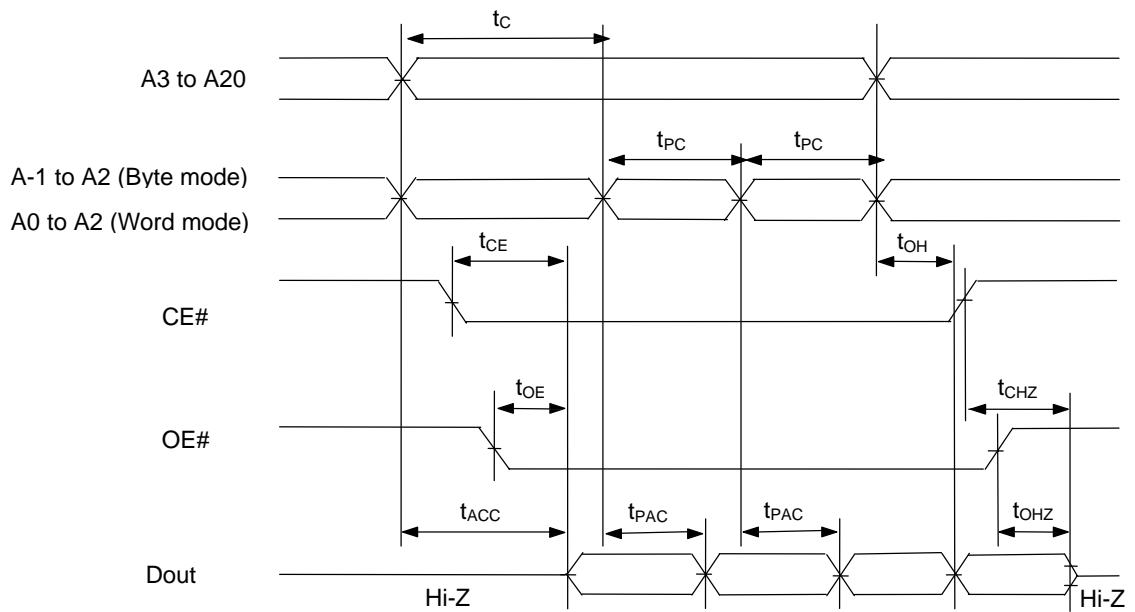


**TIMING CHART (READ CYCLE)**

**Random Access Mode Read Cycle**



**Page Access Mode Read Cycle**



**ELECTRICAL CHARACTERISTICS (PROGRAMMING OPERATION)****DC CHARACTERISTICS**

(Ta = 25°C ± 5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I <sub>LI</sub>	V <sub>I</sub> = V <sub>CC</sub> +0.5 V	—	—	10	μA
V <sub>PP</sub> power supply current (Program)	I <sub>PP2</sub>	CE# = V <sub>IL</sub>	—	—	50	mA
V <sub>CC</sub> power supply current	I <sub>CC</sub>	—	—	—	50	mA
Input "H" level	V <sub>IH</sub>	—	V <sub>CC</sub> -0.5	—	V <sub>CC</sub> +0.5	V
Input "L" level	V <sub>IL</sub>	—	-0.5	—	0.8	V
Output "H" level	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA	2.4	—	—	V
Output "L" level	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA	—	—	0.45	V
Program voltage	V <sub>PP</sub>	—	8.0	8.2	8.4	V
V <sub>CC</sub> power supply voltage	V <sub>CC</sub>	—	3.9	4.0	4.1	V

Voltage is relative to V<sub>SS</sub>.**AC CHARACTERISTICS**(V<sub>CC</sub> = 4.0 V ± 0.1 V, BYTE#/V<sub>PP</sub> = 8.2 V ± 0.25 V, Ta = 25°C ± 5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address set-up time	t <sub>AS</sub>	—	100	—	—	ns
OE# set-up time	t <sub>OES</sub>	—	2	—	—	μs
Data set-up time	t <sub>DS</sub>	—	100	—	—	ns
Address hold time	t <sub>AH</sub>	—	2	—	—	μs
Data hold time	t <sub>DH</sub>	—	100	—	—	ns
Output float delay time from OE#	t <sub>OZH</sub>	—	0	—	100	ns
V <sub>PP</sub> voltage set-up time	t <sub>VS</sub>	—	2	—	—	μs
Program pulse width	t <sub>PW</sub>	—	7	8	9	μs
Data valid from OE#	t <sub>OE</sub>	—	—	—	100	ns
Address hold from OE# high	t <sub>AOH</sub>	—	0	—	—	ns

**Pin Check Function**

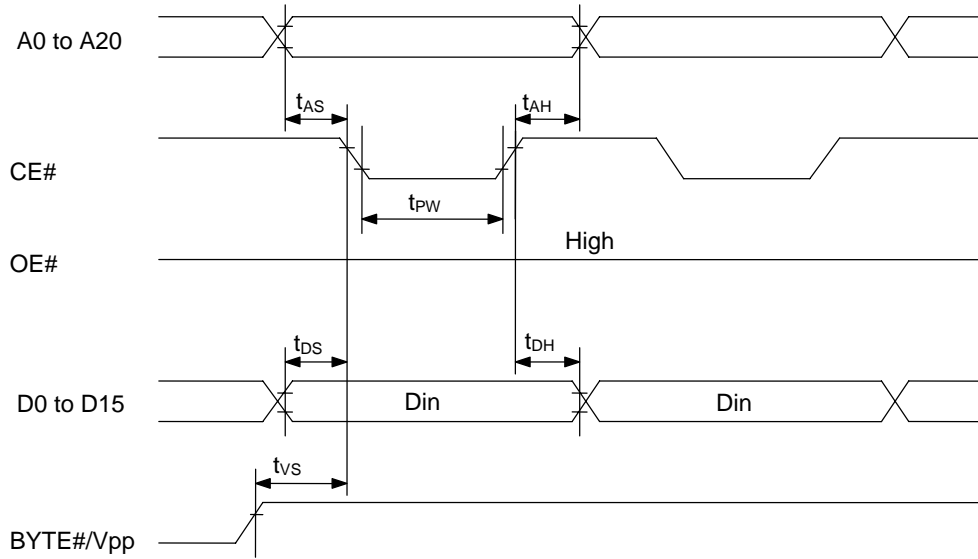
Pin Check Function is to check contact between each device-pin and each socket-lead with EPROM programmer. Setting up address as following condition call the preprogrammed codes on device outputs.

(V<sub>CC</sub> = 3.0 V ± 0.1 V, CE# = V<sub>IL</sub>, OE# = V<sub>IL</sub>, BYTE#/V<sub>PP</sub> = V<sub>IH</sub>, Ta = 25°C ± 5°C)

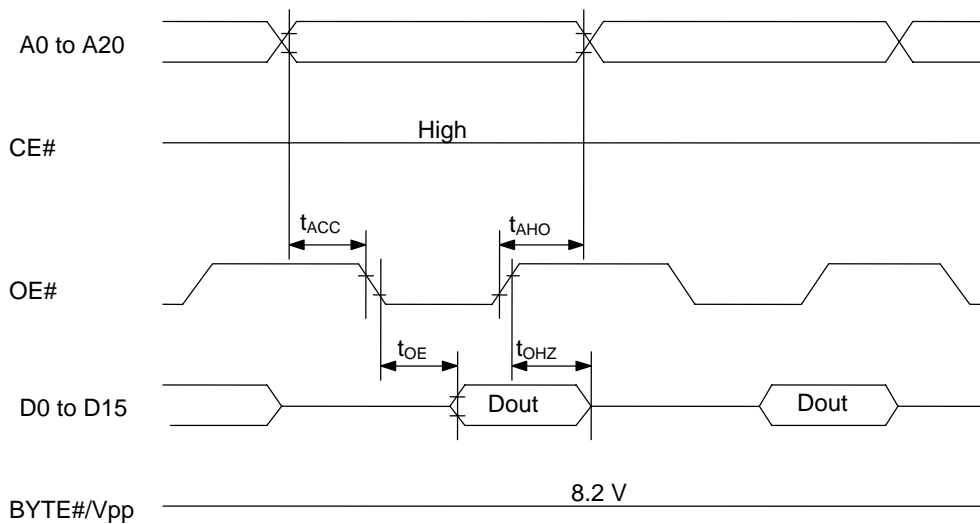
A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	DATA
0	1	0	1	0	1	0	1	0	VH	0	1	0	1	0	1	0	0	1	1	0	FF00
1	0	1	0	1	0	1	0	1	VH	1	0	1	0	1	0	1	1	0	0	1	00FF
Other conditions																				FFFF	

\*: VH = 7 V ± 0.25 V

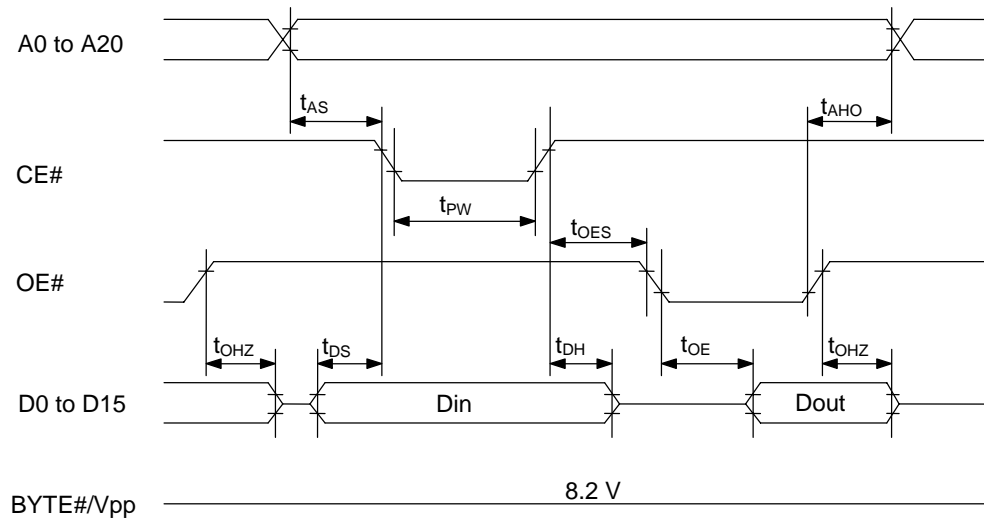
**Consecutive Programming Waveforms**



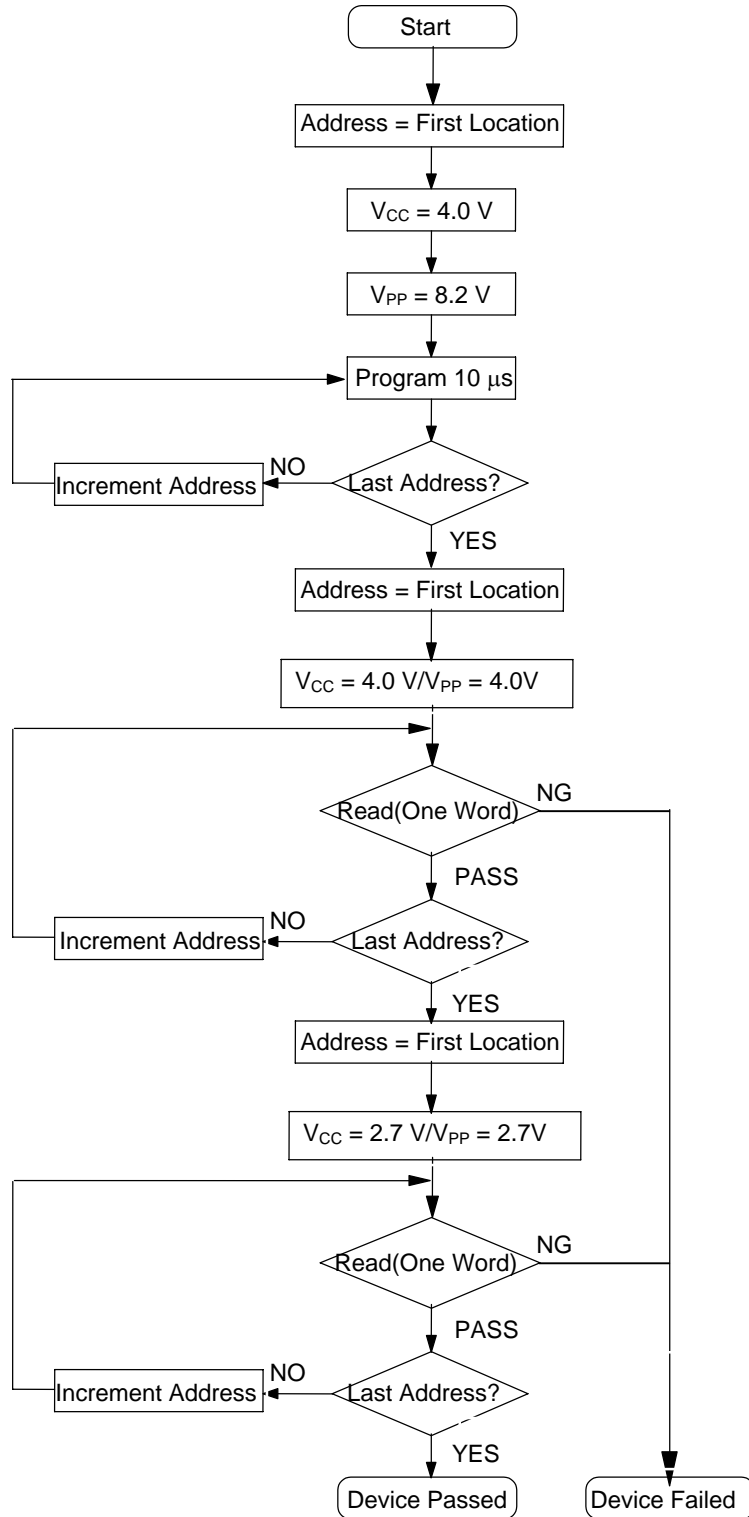
**Consecutive Program Verify Waveforms**



### Program and Program Verify Cycle Waveforms

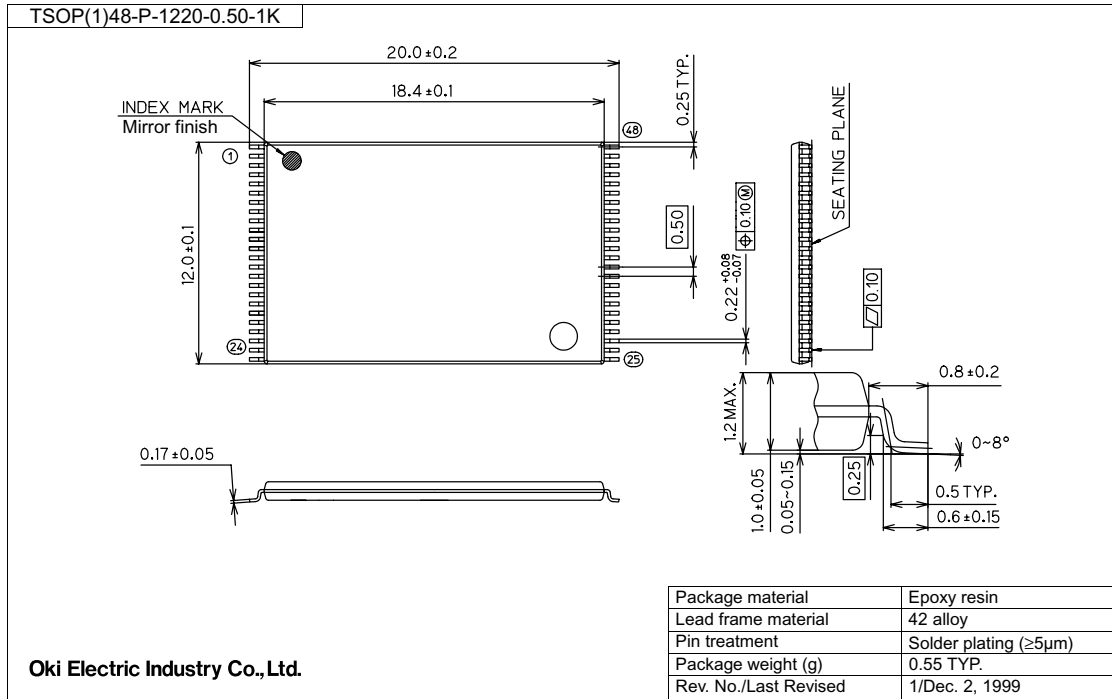


Programming Flow Chart



**PACKAGE DIMENSIONS**

(Unit: mm)



**Notes for Mounting the Surface Mount Type Package**

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR27V3252J-01-01	Mar. 26, 2004	–	–	Final edition 1
FEDR27V3252J-01-02	Jul. 9, 2004	3	3	Add P <sub>D</sub> condition and I <sub>OS</sub> = 10mA

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