FEDL610501Q501-01
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OKI Semiconductor

ML610501/ML610Q501

nX 610K CMOS 8-Bit Microcontroller (including 10-bit × 10-ch A/D converter)

GENERAL DESCRIPTION

The ML610501 is an 8-bit low-power microcontroller with a built-in high performance 10-bit A/D converter. Since the CPU core executes almost all instructions within one clock period due to a 3-stage pipeline processing, it is possible to write very efficient programs. Further, since low power consumption operation is being made due to the use of dual clocks, this microcontroller is ideally suitable for incorporation in portable equipment driven by batteries.

Furthermore, speedy product development and version upgrading can be made because a Flash ROM version(ML610Q501) that is pin-compatible with the ML610501 and programmable using a single power supply is available.

FEATURES

Type.	ML610501	ML610Q501
Operating voltage/ Operating frequency	2.7 to 3.6 V/10MHz	2.7 to 3.6 V/10MHz
	1.8 to 3.6 V/4 MHz	2.3 to 3.6 V/4 MHz
Supply current	1.5 μA (typ) @32 KHz (HALT)	
Instruction execution time	30 μs (@ 3 2 KHz system clock) 200 ns (@ 5 MHz system clock)(*1)	
ROM size	24K × 16 bits (48k bytes)	
RAM size	2K × 8 bits	
I/O port	8 input ports	
	33 I/O ports	
Timer	8-bit × 4ch	
	Watch dog timer	
Serial port	I^2C × 2ch	
	UART × 1ch	
	Synchronous × 1ch	
A/D converter	10-bit × 10ch	
PWM	16-bit × 1	
External interrupt	8	
Internal interrupt	Timer × 4, Time base counter × 4 I^2C × 2, UART × 1, Synchronous × 1 PWM × 1, Watch dog timer × 1 A/D converter × 1	
Low speed clock	32 KHz (crystal oscillator, RC oscillator)	
Temperature range	–20 to 70°C	

*1 The system clock should be set to a value below 5 MHz by the built-in divided clock circuit.

APPLICATIONS

Digital Camera, AV portable machines, etc.

PACKAGE

64PIN BGA (7mm × 7mm) 64PIN BGA (6mm × 6mm)

BLOCK DIAGRAM

The block diagram of the ML610501 is shown in Fig. 1

An asterisk "*" indicates the secondary function of each port.

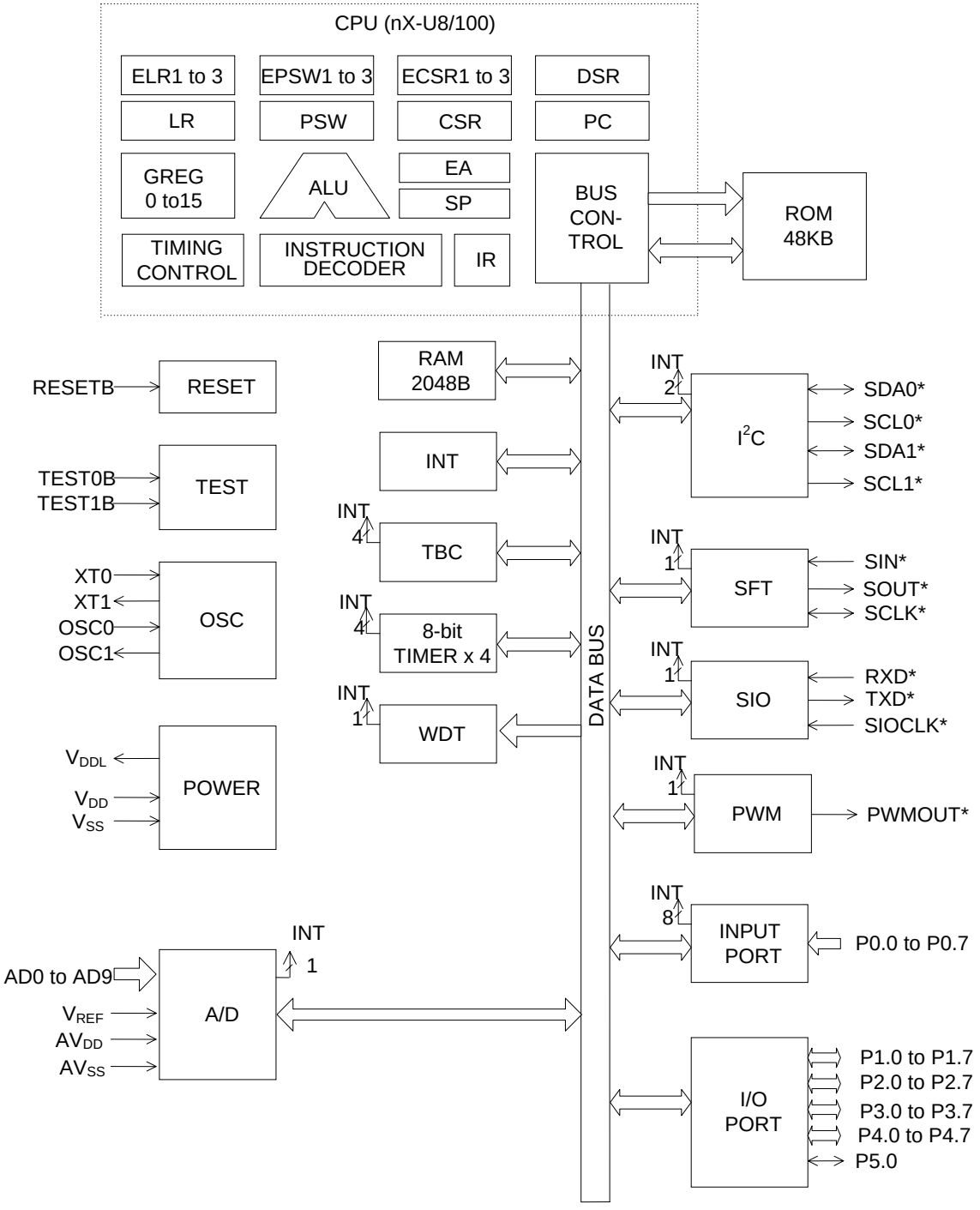


Figure 1 ML610501 Block Diagram

PIN CONFIGURATION (BOTTOM VIEW)

The pin configuration of the ML610501 is shown in Fig. 2.

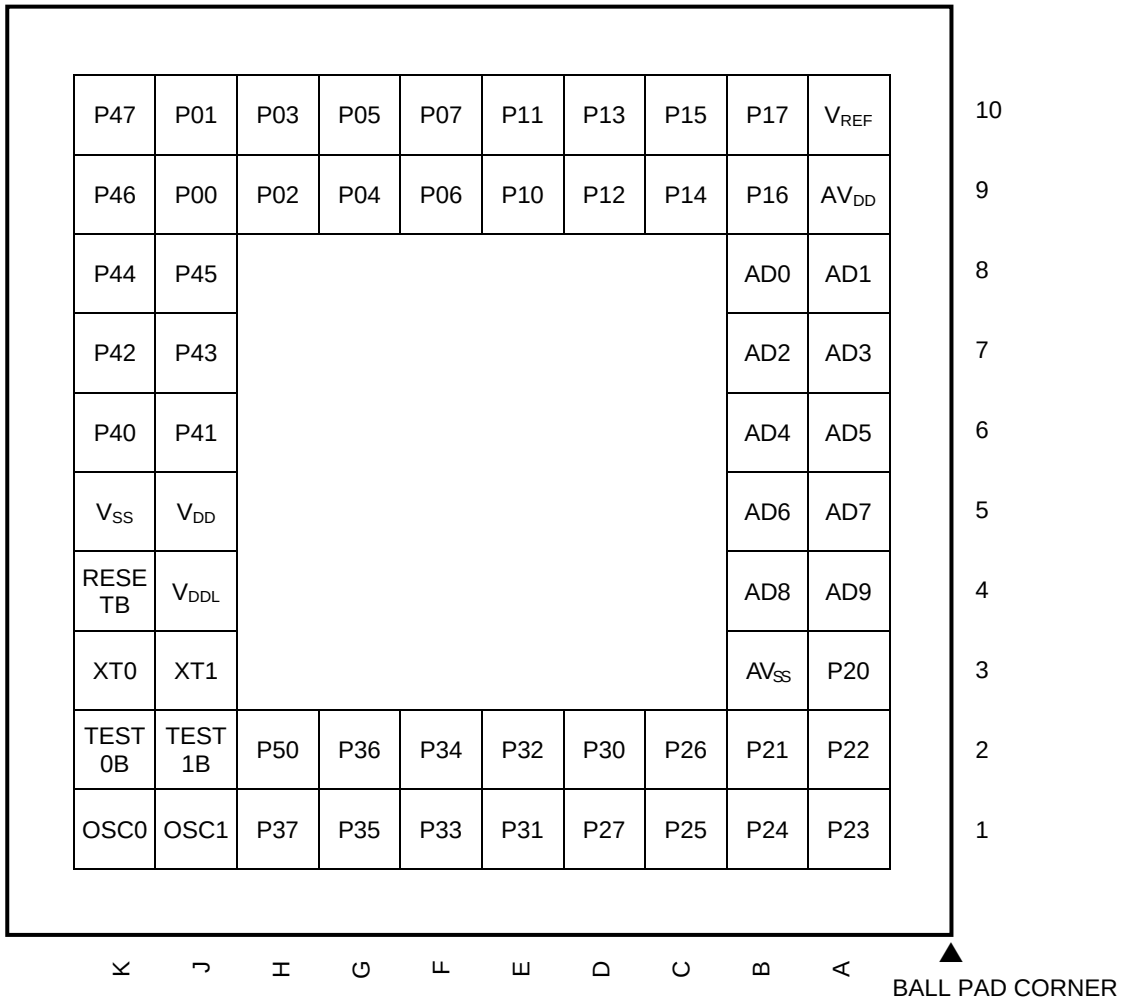
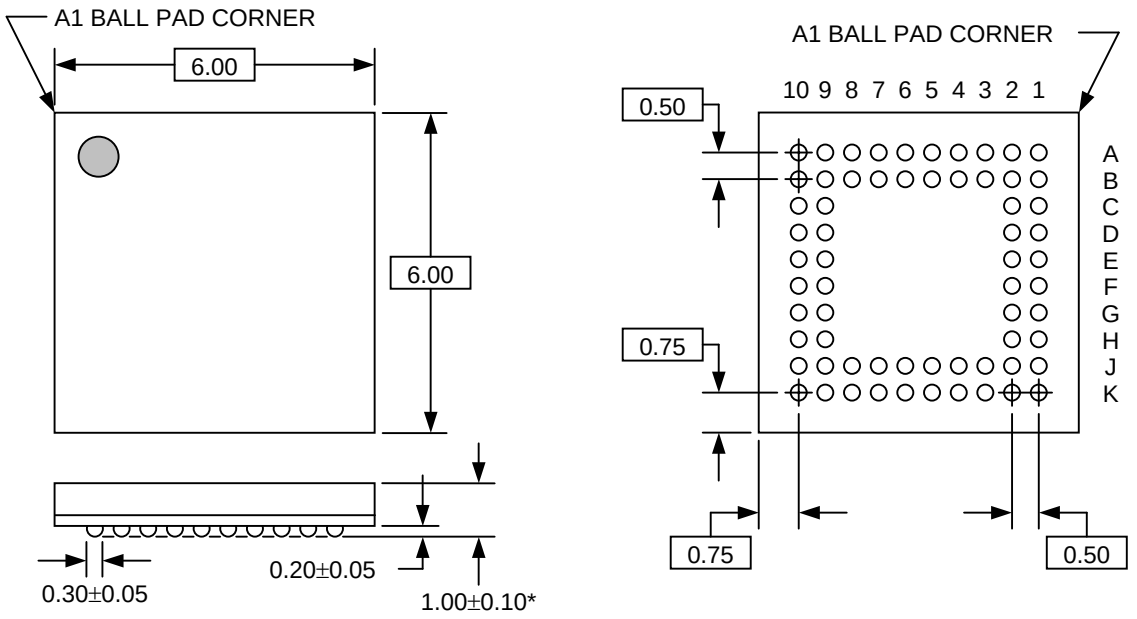


Figure 2 ML610501 Pin Configuration

PACKAGE DIMENSIONS

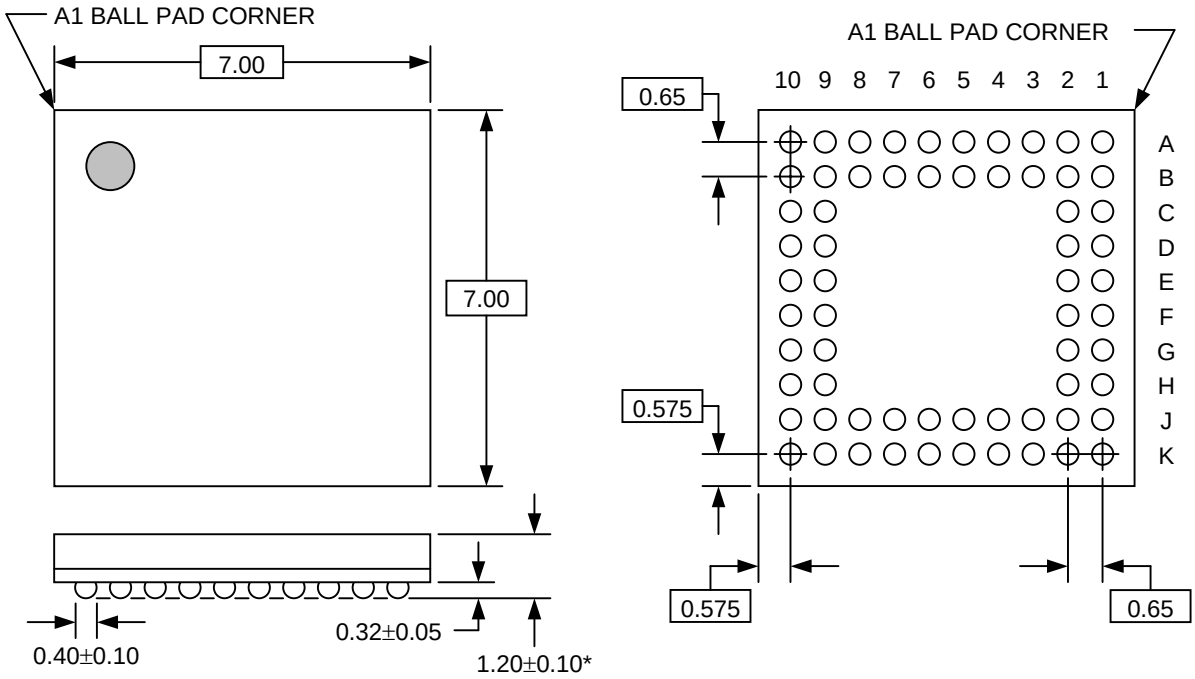
ML610501-xxxLA, ML610Q501-XxxxLA (6 mm × 6 mm)



*:1.10±0.10 for ML610Q501

Figure 3-1 BGA64-0606-0.50

ML610501-xxxLP, ML610Q501-XxxxLP (7 mm × 7 mm)



*:1.30±0.10 for ML610Q501

Figure 3-2 BGA64-0707-0.65

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (ML610501/Q501)

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 2	V_{DDL}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 3	AV_{DD}	Ta = 25°C	–0.3 to +4.6	V
Input voltage 1	V_{IN1}	V_{DD} input, Ta = 25°C	–0.3 to V_{DD} +0.3	V
Output voltage 1	V_{OUT1}	V_{DD} output, Ta = 25°C	–0.3 to V_{DD} +0.3	V
Output voltage 2	V_{OUT2}	V_{DDL} output, Ta = 25°C	–0.3 to V_{DDL} +0.3	V
Power dissipation	P_D	Ta = –20 to 70°C	200	mW
Storage temperature	T_{STG}	—	–55 to +150	°C

Recommended Operating Conditions (ML610501/Q501)

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	–20 to +70	°C
Operating voltage	V_{DD}	ML610501	1.8 to 3.6	V
	V_{DD}	ML610Q501	2.3 to 3.6	
	AV_{DD}	—	1.8 to 3.6	
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.8 to 3.6 V	30 k to 2.048 M	Hz
		V_{DD} = 2.7 to 3.6 V	30 k to 5 M	
Low-speed crystal oscillator frequency	f_{XTL}	—	32.768 k	Hz
Low-speed RC oscillator frequency	f_{CRL}	—	30 k to 100 k	Hz
Low-speed External clock frequency	f_{EXL}	—	30 k to 100 k	Hz
High-speed crystal/ceramic oscillator frequency	f_{XTH}	V_{DD} = 1.8 to 3.6 V	1 M to 4.096 M	Hz
		V_{DD} = 2.7 to 3.6 V	1 M to 10 M	
High-speed external clock frequency	f_{ETH}	—	30 k to 10 M	Hz
High-speed RC oscillator frequency	f_{CRH}	—	400 k to 2 M	Hz

Flash ROM Operating Conditions (ML610Q501)

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	During reading	–20 to +70	°C
		During writing	0 to +70	
Operating voltage	V_{DD}	—	2.3 to 3.6	V
Program cycles	C_{EP}	—	100	Cycle

DC Characteristics (ML610501/Q501)

(V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
V_{DDL} voltage	V_{DDL}	High-speed oscillation stopped	1.2	1.6	2.2	V	1
		At reset or in high-speed oscillation	—	V_{DD}	—		
Low-speed crystal oscillation start time	T_{XTL}	—	—	—	2	s	
External capacitor for low-speed crystal oscillator	C_{DL}	—	10	18	47	pF	
	C_{GL}	—	5	15	33		
Low-speed RC oscillation frequency	f_{CRL}	R_{OSL} = 300kΩ ±5%	30	50	100	kHz	
Hi-speed crystal/ceramic oscillation start time	T_{XTH}	—	—	—	20	ms	
External capacitor for high-speed crystal oscillator/ceramic resonator	C_{DH}	—	5	5	56	pF	
	C_{GH}	—	5	20	56		
High-speed RC oscillation frequency	f_{CRH}	R_{OSH} = 200kΩ ±5%	400 k	700 k	2 M	Hz	
Low-speed oscillation stop detection time (*1)	T_{STOP}	—	0.2	3	20	ms	
Power-on reset generation voltage	V_{POR1}	V_{DD} = 3.0 V	0	—	0.7	V	
Power-on reset non-generation voltage	V_{POR2}	V_{DD} = 3.0 V	1.8	—	3.0		
Power-on reset generation power-up time	T_{POR}	V_{DD} = 3.0 V	—	—	100	μs	

*1 The system reset mode is entered if low-speed oscillation stops for a longer period than this time.

DC Characteristics (ML610501: Mask ROM Version)

(V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	I_{DD1}	STOP state		—	0.4	2	μA	1
Supply current 2	I_{DD2}	HALT state High-speed clock stopped	Crystal oscillation circuit (32.768 kHz)	—	1.5	4		
			RC oscillation circuit (ROSL = 300 kΩ)	—	17	35		
			External clock input (32.768 kHz)	—	2	5		
Supply current 3	I_{DD3}	CPU operating at low speed High-speed clock stopped	Crystal oscillation circuit (32.768 kHz)	—	6	12		
			RC oscillation circuit (ROSL = 300 kΩ)	—	24	45		
			External clock input (32.768 kHz)	—	6.5	13		
Supply current 4	I_{DD4}	CPU operating at high speed (5 MHz) High-speed clock in oscillation (10 MHz ceramic resonator)		—	1.2*	2.5	mA	

*1 Condition : V_{DD} = 3.0 V

DC Characteristics (ML610Q501: Flash ROM Version)

(V_{DD} = 2.3 to 3.6 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	I_{DD1}	STOP state		—	0.8	50	μA	1
Supply current 2	I_{DD2}	HALT state High-speed clock stopped	Crystal oscillation circuit (32.768 kHz)	—	2	50		
			RC oscillation circuit (ROSL = 300 kΩ)	—	18	65		
			External clock input (32.768 kHz)	—	2.5	50		
Supply current 3	I_{DD3}	CPU operating at low speed High-speed clock stopped	Crystal oscillation circuit (32.768 kHz)	—	50*	500		
			RC oscillation circuit (ROSL = 300 kΩ)	—	65*	500		
			External clock input (32.768 kHz)	—	50*	500		
Supply current 4	I_{DD4}	CPU operating at high speed (5 MHz) High-speed clock in oscillation (10 MHz ceramic resonator)		—	7.5*	15	mA	

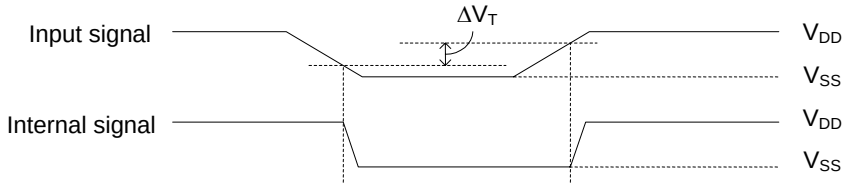
*1 Condition : V_{DD} = 3.0 V

DC Characteristics (ML610501/Q501)

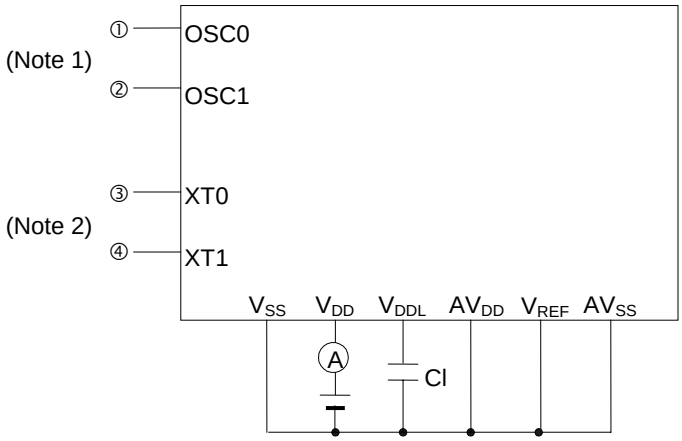
(V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Output current 1 (P1.0 to P1.7) (P2.0 to P2.7) (P3.0 to P3.7) (P4.0 to P4.7) (P5.0)	I_{OH1}	$V_{OH1} = V_{DD}$ –0.5 V	–10	–3.0	–0.5	mA	2
	I_{OL1}	V_{OL1} = +0.5 V	0.5	3.0	10		
Output current 2 (P4.0 to P4.7)	I_{OL2}	V_{OL2} = +0.5 V (when LED-driving mode is selected)	5.0	20	—		
Output leakage current (P1.0 to P1.7) (P2.0 to P2.7) (P3.0 to P3.7) (P4.0 to P4.7) (P5.0)	I_{OOH}	$V_{OH} = V_{DD}$ (at high impedance)	—	—	1	μA	
	I_{OOL}	$V_{OL} = V_{SS}$ (at high impedance)	–1	—	—		
Input current 1 (RESETB)	I_{IH1}	$V_{IH1} = V_{DD}$	—	—	1	μA	3
	I_{IL1}	$V_{IL1} = V_{SS}$	–1500	–300	–20		
Input current 2 (TEST0,1B)	I_{IH2}	$V_{IH2} = V_{DD}$	—	—	1		
	I_{IL2}	$V_{IL2} = V_{SS}$	–3000	–600	–40		
Input current 3 (P0.0 to P0.7) (P1.0 to P1.7) (P2.0 to P2.7) (P3.0 to P3.7) (P4.0 to P4.7) (P5.0)	I_{IH3}	$V_{IH3} = V_{DD}$ (when pulled down)	2	30	200		
	I_{IL3}	$V_{IL3} = V_{SS}$ (when pulled up)	–200	–30	–2		
	I_{IH3Z}	$V_{IH3} = V_{DD}$ (at high impedance)	—	—	1		
	I_{IL3Z}	$V_{IL3} = V_{SS}$ (at high impedance)	–1	—	0		
Input voltage (RESETB) (TEST0, 1B) (P0.0 to P0.7) to (P4.0 to P4.7) (P5.0)	V_{IH}	V_{DD} = 3 V	2.4	—	3.0	V	4
	V_{IL}	V_{DD} = 3 V	0.0	—	0.6		
Hysterics width(RESETB) (TEST0, 1B) (P0.0 to P0.7) to (P4.0 to P4.7) (P5.0)	ΔV_T	V_{DD} = 3 V	0.2	0.5	1.0	V	
Input pin capacitance (P0.0 to P0.7) to (P4.0 to P4.7) (P5.0)	C_{IN}	—	—	—	5	pF	—

Hysteresis Width

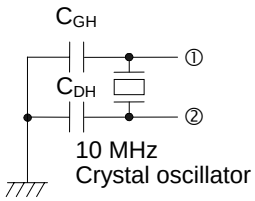


Measuring circuit 1

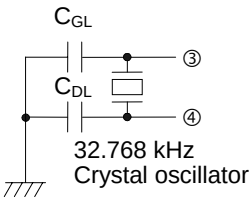


Cl: 0.47 μF
C_{GL}: 18 pF
C_{DL}: 27 pF
C_{GH}: 8 pF
C_{DH}: 8 pF

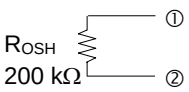
(Note 1)
Crystal oscillation



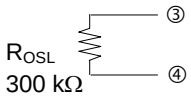
(Note 2)
Crystal oscillation



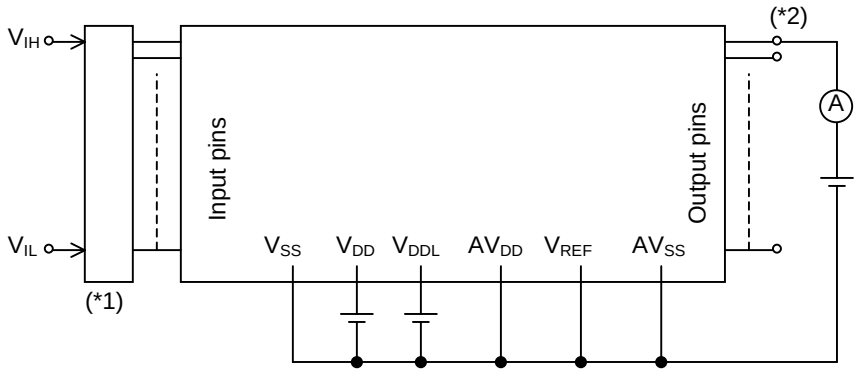
RC oscillation



RC oscillation

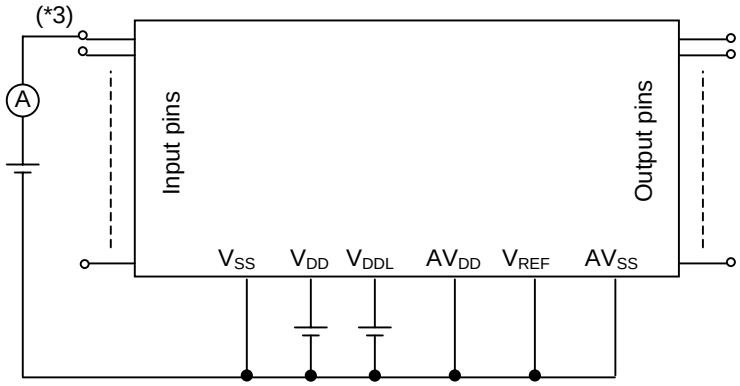


Measuring circuit 2

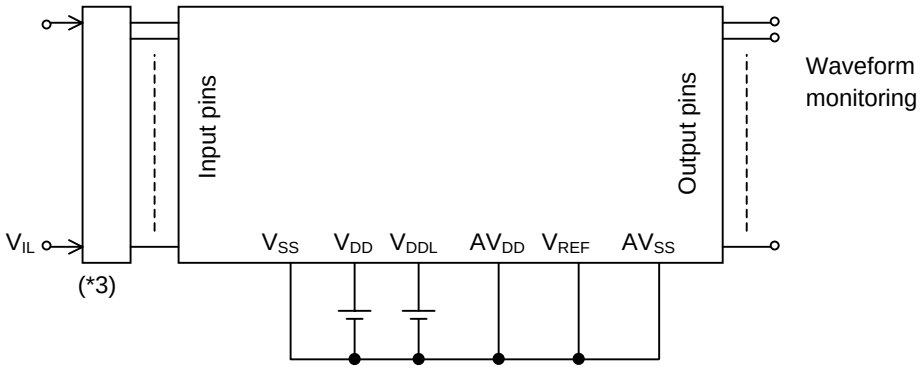


*1 Input logic circuit to select the specified measuring conditions
*2 Measured at the specified output pins

Measuring circuit 3



Measuring circuit 4

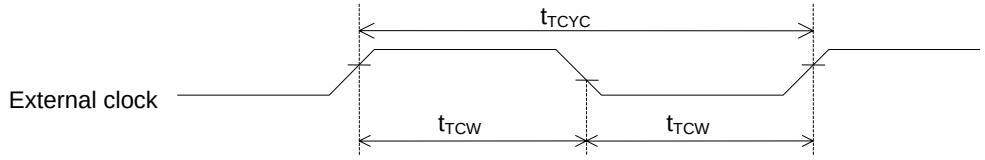


*3 Measured at the specified input pins

AC Characteristics (Timer)

(V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External clock input cycle time	t_{TCYC}	—	500	—	—	ns
External clock input pulse width	t_{TCW}	—	200	—	—	ns

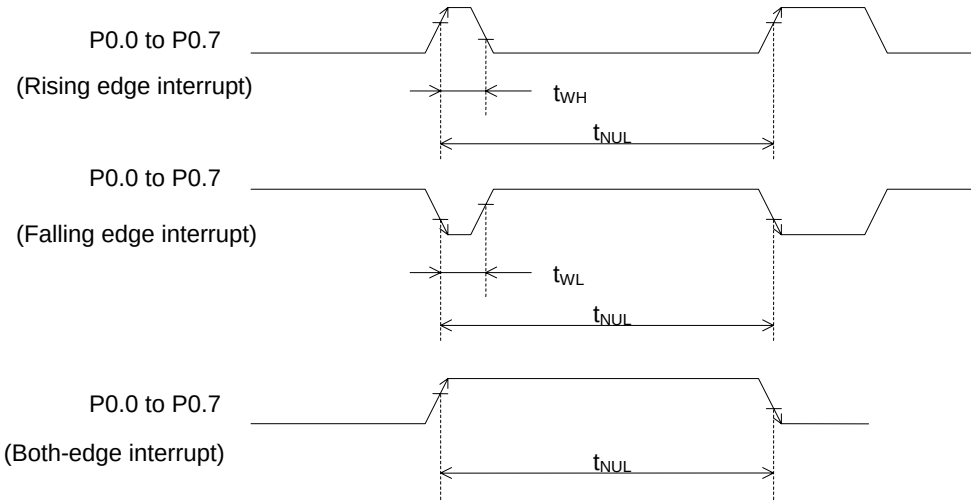


AC Characteristics (External Interrupt)

(V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt enable pulse width (rising edge)	t_{WH}	—	20	—	—	ns
External interrupt enable pulse width (falling edge)	t_{WL}	—	20	—	—	ns
External interrupt disable period	t_{NUL}	Interrupt enable, MIE = 1 CPU: NOP System clock: 32.768 kHz	91.5	—	122.1	μs

AC Characteristics (Timer)

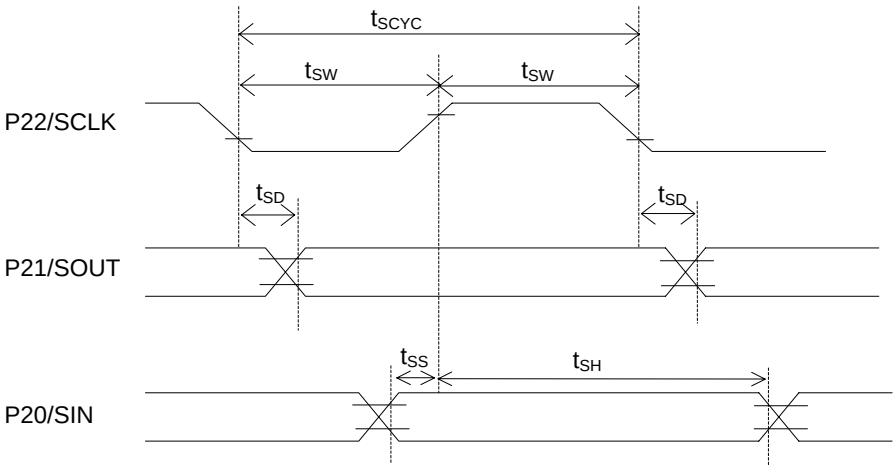


AC Characteristics (Shift Register)

(V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
SCLK input cycle (slave mode)	t_{SCYC}	High-speed oscillation stopped		10	—	—	µs
		In high-speed oscillation	V_{DD} = 1.8 to 3.6 V	500	—	—	ns
			V_{DD} = 2.7 to 3.6 V	200	—	—	
SCLK output cycle (master mode)	t_{SCYC}	—		—	SCLK*	—	s
SCLK input pulse width (slave mode)	t_{SW}	High-speed oscillation stopped		4	—	—	µs
		In high-speed oscillation	V_{DD} = 1.8 to 3.6 V	200	—	—	ns
			V_{DD} = 2.7 to 3.6 V	80	—	—	
SCLK output pulse width (master mode)	t_{SW}	—		SCLK* × 0.4	SCLK* × 0.5	SCLK* × 0.6	s
SOUT output delay time	t_{SD}	V_{DD} = 1.8 to 3.6 V		—	—	100	ns
		V_{DD} = 2.7 to 3.6 V		—	—	50	
SIN input setup time	t_{SS}	V_{DD} = 1.8 to 3.6 V		100	—	—	ns
		V_{DD} = 2.7 to 3.6 V		50	—	—	
SIN input hold time	t_{SH}	V_{DD} = 1.8 to 3.6 V		100	—	—	ns
		V_{DD} = 2.7 to 3.6 V		50	—	—	

*SCLK: Clock period selected by SFCK3 to 0 of shift register mode register (SFTMOD)

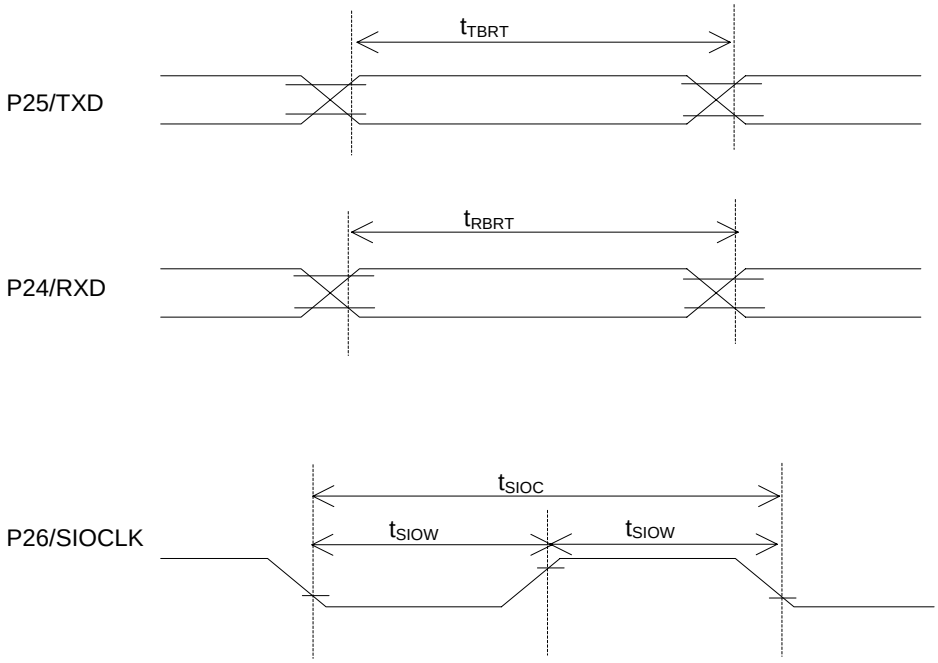


AC Characteristics (Serial Port)

(V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit baud rate	t_{TBRT}	—	—	BRT*	—	s
Receive baud rate	t_{RBRT}	—	BRT* × 0.97	BRT*	BRT* × 1.03	s
SIOCLK input cycle	t_{SIOC}	—	500	—	—	ns
SIOCLK input pulse width	t_{SIOW}	—	200	—	—	ns

*BRT: The baud rate period set by the serial port baud rate regisgers (SIOBRTL, SIOBRTH) and serial port mode register 0 (SIOMODO) (including errors of the selected clock frequencies)



AC Characteristics (I^2C Bus Interface: Standard Mode 100 kHz)

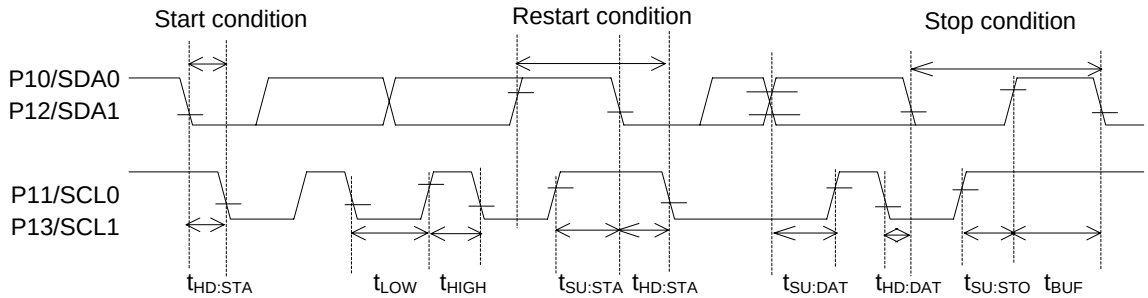
(V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL cycle	t_{SCL}	Clock synchronization function disabled	—	10	—	µs
SCL "L" level pulse width	t_{LOW}	—	—	5.5	—	µs
SCL "H" level pulse width	t_{HIGH}	Clock synchronization function enabled	—	4.5	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	Clock synchronization function enabled	—	4.5	—	µs
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	—	4.5	—	µs
SDA setup time	$t_{HD:DAT}$	Data transmit mode	—	5.0	—	µs
		Data receive mode	0.2	—	—	
SDA hold time	$t_{SU:DAT}$	Data transmit mode	—	5.0	—	µs
		Data receive mode	0	—	3.5	
SDA setup time (stop condition)	$t_{SU:STO}$	Clock synchronization function enabled	—	4.5	—	µs
Bus free time	t_{BUF}	—	—	5.5	—	µs

AC Characteristics (I^2C Bus Interface: Fast Mode 400 kHz)

(V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

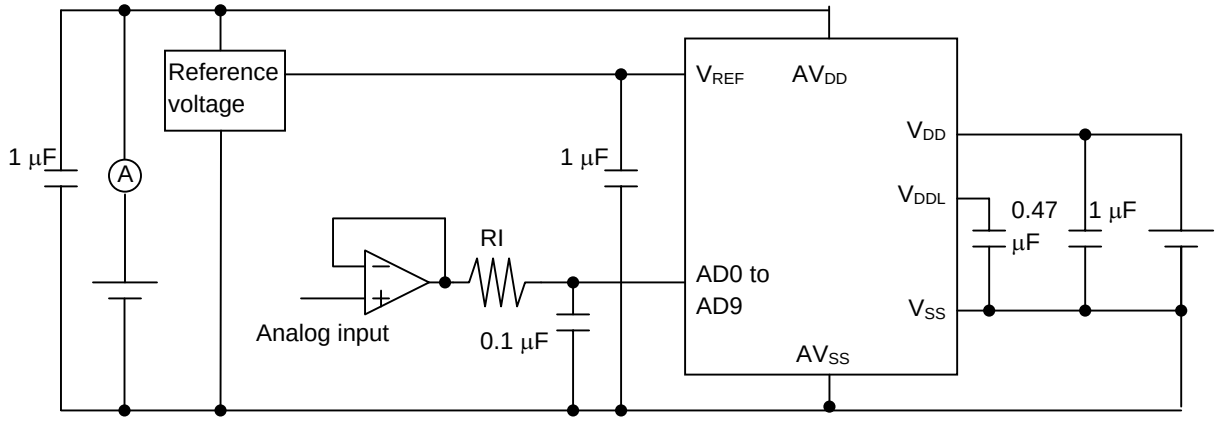
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL cycle	t_{SCL}	Clock synchronization function disabled	—	2.5	—	µs
SCL "L" level pulse width	t_{LOW}	—	—	1.5	—	µs
SCL "H" level pulse width	t_{HIGH}	Clock synchronization function enabled	—	1.0	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	Clock synchronization function enabled	—	1.0	—	µs
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	—	1.0	—	µs
SDA setup time	$t_{HD:DAT}$	Data transmit mode	—	1.0	—	µs
		Data receive mode	0.2	—	—	
SDA hold time	$t_{SU:DAT}$	Data transmit mode	—	0.5	—	µs
		Data receive mode	0	—	1.0	
SDA setup time (stop condition)	$t_{SU:STO}$	Clock synchronization function enabled	—	1.0	—	µs
Bus free time	t_{BUF}	—	—	1.5	—	µs



A/D Converter Electrical Characteristics (ML610501/Q501)

(AV_{DD} = 1.8 to 3.6 V, AV_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Analog input impedance RI ≤ 5 kΩ	—	—	10	bit
Linearity error	EL		—	—	3.0	LSB
Differential linearity error	ED		—	—	2.0	
Offset error	EO		—	—	2.0	
Overall error	EA	2.3 V ≥ V_{REF} ≥ 1.8 V	—	—	±4.0	
		3.6 V ≥ V_{REF} > 2.3 V	—	—	±3.0	
Reference voltage	V_{REF}	—	1.8	—	AV_{DD}	V
Conversion time	t_{CONV}	Conversion clock: 5 MHz	—	8.0	—	µs/CH
		Conversion clock: 32.768 KHz	—	732	—	
Supply current	IDAD	When ADC is operating at AV_{DD} = 1.8 V	—	0.7	1.5	mA
		When ADC is operating at AV_{DD} = 3.0 V	—	3.5	5	
		When ADC is operating at AV_{DD} = 3.6 V	—	5.8	8	
	IDAS	When ADC is stopped (but AV_{DD} is applied)	—	—	1	µA



MASK OPTIONS

List of ML610501 Mask Options

Address	Function	Mask option selection data		
0BF00H	Low-speed oscillation circuit	0000H: Crystal oscillation circuit	0001H: RC oscillation circuit	0002H: External clock input
0BF02H	Reset format & low-speed oscillation stop detection reset	0000H: Direct & disabled (not used).	0001H: Direct & enabled (used).	0002H: Sampling & enabled (used)

Assign these mask option data to addresses 0BF00h and 0BF02H in the test data area. The set data cannot be used for applications programs.
The reset sampling clock is LSCLK (32.768 kHz).
In the ML610Q501 flash ROM version, it is not necessary to set the mask option data.

[Example of mask option data creation]
To select the crystal oscillation circuit and to use reset sampling & low-speed oscillation stop detection reset, assign the data as follows:

```
CSEG    AT      0:0BF00H
DW      0000H   ; Select the crystal oscillation circuit.
DW      0002H   ; Use reset sampling & low-speed oscillation stop detection reset.
```

List of ML610Q501-Xxxx Mask Option Codes

X: Mask option code
xxx: programed code number NNN means brank version

Mask option code	Mask option select function	
	Low-speed oscillation circuit	Reset format & low-speed oscillation stop detection reset
1	Crystal oscillation circuit	Sampling & enabled (used)
2	RC oscillation circuit	
3	External clock input	
4	Crystal oscillation circuit	Direct & disabled (not used)
5	RC oscillation circuit	
6	External clock input	

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610501Q501-01	Dec. 17, 2003	–	–	Final edition 1

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