

GENERAL DESCRIPTION

The ML87V21071, which comprises a frame memory and signal processing and memory control logic circuits, has achieved motion-adaptive 3D noise reduction.

To perform noise reduction with afterimage suppression, the ML87V21071 also enables noise reduction using the edge-adaptive 2D noise reduction filter.

Each noise reduction function allows setting an automatic mode. In automatic mode, noise of a vertical blanking period and a valid data period is detected to reduce noise according to the noise status from which the noise reduction setting value is detected.

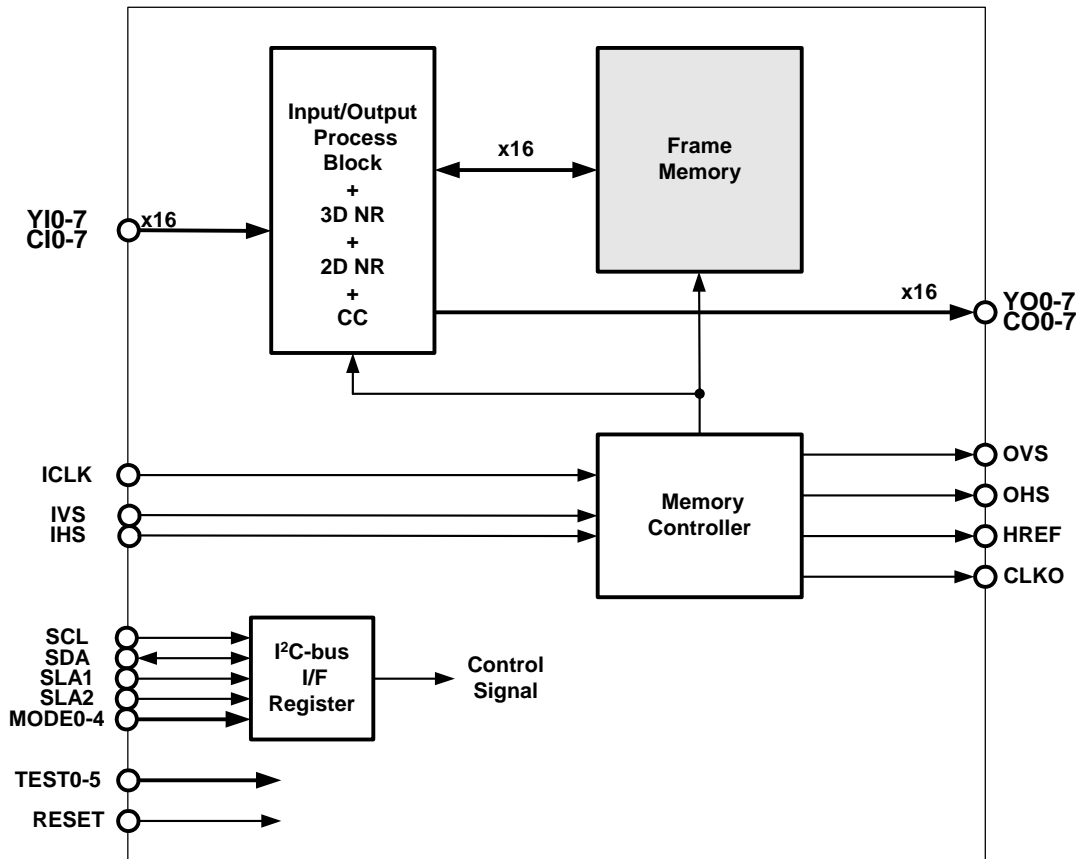
The ML87V21071 also has a cross-color cancellation function that uses the motion-adaptive 3D comb filter method that removes cross colors occurring at two-dimensional YC separation in the NTSC/PAL system.

Since the same format as the input can be selected for output, noise reduction can easily be achieved by inserting the IC into the conventional system.

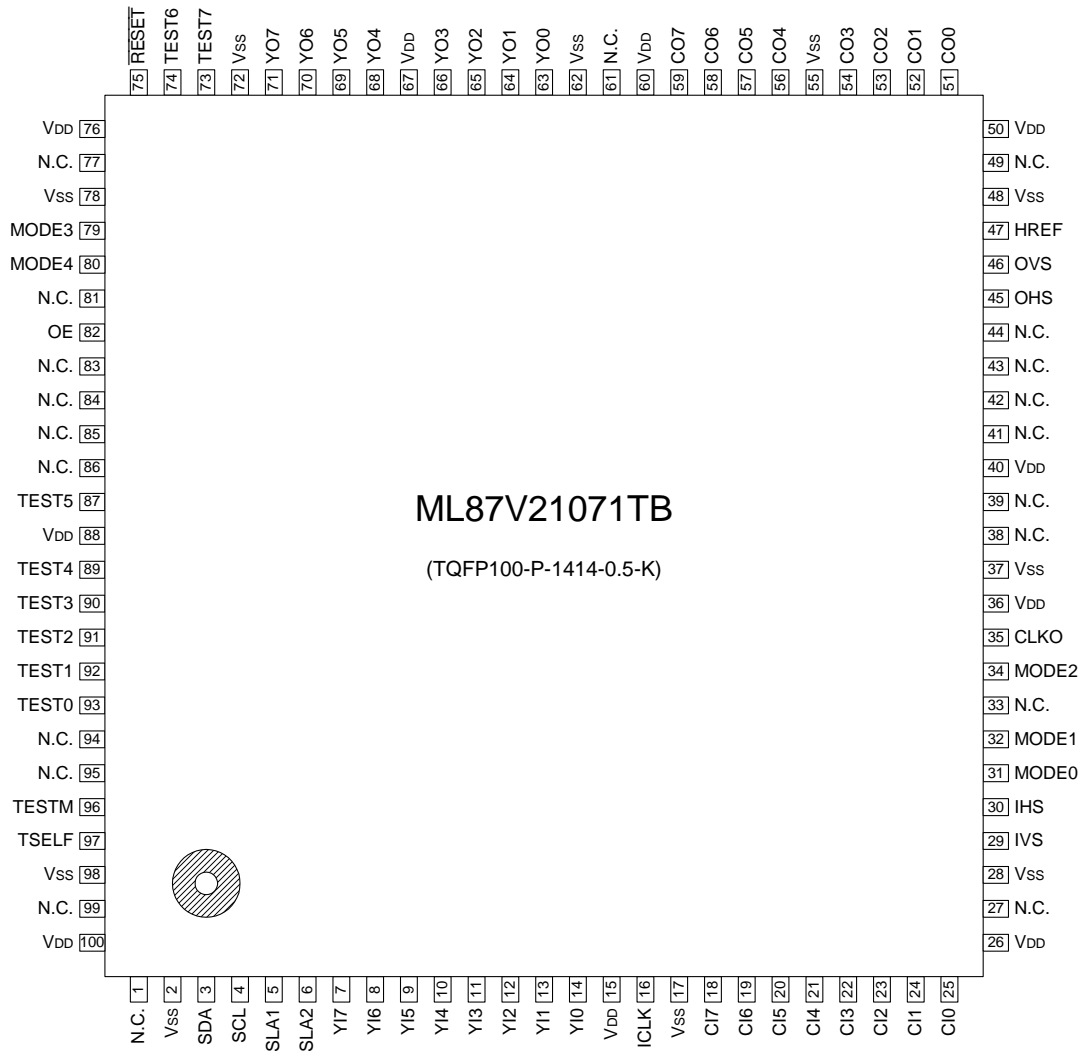
FEATURES

- Built-in memory:
Frame memory (78 × 608 × 16-bit) × 1 unit
- Maximum input and output operating frequencies (16-bit/8-bit, ITU-R BT.656):
14.75/29.5 MHz
* For 525p/625p, only 16-bit input mode is supported (Max.: 29.5 MHz).
- Power supply voltage:
3.3 V ± 0.3 V
- Input/output pin:
LVCMOS (3.3 V)
- Input/output data format:
YCbCr (8 bit (Y) + 8 bit (CbCr))(4:2:2): 16-bit mode
YCbCr (8 bit (YCbCr))(4:2:2): 8-bit mode
ITU-R656 (8 bit (YCbCr)): ITU-R BT.656 mode
* In 16-bit input mode, neither 8-bit mode nor ITU-R BT.656 mode can be selected for output.
- Serial bus:
I²C-bus interface: (400 kHz, 100 kHz)
- Memory controller:
Compatible with 625/50Hz 2:1(625i), 525/60Hz 2:1(525i), 625/50Hz 1:1(625p), and 525/60Hz 1:1(525p)
- Motion-adaptive 3D noise reduction:
Frame-field-line-correlation noise detection and noise subtraction method
Supports automatic noise reduction setting
- Edge-adaptive 2D noise reduction:
Edge-adaptive space filter used
- Chrominance signal cross color cancelling:
Motion-adaptive 3D comb filter used
Compatible with 525i (NTSC decode signal)/625i (PAL decode signal)
- Package:
100-pin TQFP (TQFP100-P-1414-0.50-K) (ML87V21071TB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTIONS

No.	Symbol	I/O	Pad Remarks	Pin Description	Termination of unused pin
1	N.C.	—		Unused pin	Not used
2	V _{SS}	—		Ground	X
3	SDA	I/O	Schmitt(IN)/ OpenDrain(OUT)	I ² C-bus data pin	X
4	SCL	I	Schmitt	I ² C-bus clock pin	X
5	SLA1	I	Schmitt pull-down 50k	Slave address setting pin bit 1	Not used or connected to GND
6	SLA2	I	Schmitt pull-down 50k	Slave address setting pin bit 2	Not used or connected to GND
7	YI7	I		Luminance signal input pin bit 7 (MSB)	X
8	YI6	I		Luminance signal input pin bit 6	X
9	YI5	I		Luminance signal input pin bit 5	X
10	YI4	I		Luminance signal input pin bit 4	X
11	YI3	I		Luminance signal input pin bit 3	X
12	YI2	I		Luminance signal input pin bit 2	X
13	YI1	I		Luminance signal input pin bit 1	X
14	YI0	I		Luminance signal input pin bit 0 (LSB)	X
15	V _{DD}	—		3.3 V power supply	X
16	ICLK	I		System clock Input pin	X
17	V _{SS}	—		Ground	X
18	CI7	I	pull-down 50k	Chrominance signal input pin bit 7 (MSB)	Not used or connected to GND
19	CI6	I	pull-down 50k	Chrominance signal input pin bit 6	Not used or connected to GND
20	CI5	I	pull-down 50k	Chrominance signal input pin bit 5	Not used or connected to GND
21	CI4	I	pull-down 50k	Chrominance signal input pin bit 4	Not used or connected to GND
22	CI3	I	pull-down 50k	Chrominance signal input pin bit 3	Not used or connected to GND
23	CI2	I	pull-down 50k	Chrominance signal input pin bit 2	Not used or connected to GND
24	CI1	I	pull-down 50k	Chrominance signal input pin bit 1	Not used or connected to GND
25	CI0	I	pull-down 50k	Chrominance signal input pin bit 0 (LSB)	Not used or connected to GND
26	V _{DD}	—		3.3 V power supply	X
27	N.C.	—		Unused pin	Not used
28	V _{SS}	—		Ground	X
29	IVS	I	Schmitt pull-down 50k	Input system vertical Sync. signal input pin	Not used or connected to GND
30	IHS	I	Schmitt pull-down 50k	Input system horizontal Sync. signal input pin	Not used or connected to GND
31	MODE0	I	Schmitt pull-down 50k	Mode setting pin bit 0 (Equivalent to internal register VMD[0])	Not used or connected to GND
32	MODE1	I	Schmitt pull-down 50k	Mode setting pin bit 1 (Equivalent to internal register HMD[0])	Not used or connected to GND
33	N.C.	—		Unused pin	Not used

No.	Symbol	I/O	Pad Remarks	Pin Description	Termination of unused pin
34	MODE2	I	Schmitt pull-down 50k	Mode setting pin bit 2 (Equivalent to internal register DISEL[0])	Not used or connected to GND
35	CLKO	O		Clock output (I ² C-bus control possible)	Not used
36	V _{DD}	—		3.3 V power supply	X
37	V _{SS}	—		Ground	X
38	N.C.	—		Unused pin	Not used
39	N.C.	—		Unused pin	Not used
40	V _{DD}	—		3.3 V power supply	X
41	N.C.	—		Unused pin	Not used
42	N.C.	—		Unused pin	Not used
43	N.C.	—		Unused pin	Not used
44	N.C.	—		Unused pin	Not used
45	OHS	O		Horizontal Sync. signal output pin	Not used
46	OVS	O		Vertical Sync. signal output pin	Not used
47	HREF	O		Data output horizontal reference signal output pin	Not used
48	V _{SS}	—		Ground	X
49	N.C.	—		Unused pin	Not used
50	V _{DD}	—		3.3 V power supply	X
51	CO0	O		Chrominance signal output pin bit 0 (LSB)	Not used
52	CO1	O		Chrominance signal output pin bit 1	Not used
53	CO2	O		Chrominance signal output pin bit 2	Not used
54	CO3	O		Chrominance signal output pin bit 3	Not used
55	V _{SS}	—		Ground	X
56	CO4	O		Chrominance signal output pin bit 4	Not used
57	CO5	O		Chrominance signal output pin bit 5	Not used
58	CO6	O		Chrominance signal output pin bit 6	Not used
59	CO7	O		Chrominance signal output pin bit 7 (MSB)	Not used
60	V _{DD}	—		3.3 V power supply	X
61	N.C.	—		Unused pin	Not used
62	V _{SS}	—		Ground	X
63	YO0	O		Luminance signal output pin bit 0 (LSB)	X
64	YO1	O		Luminance signal output pin bit 1	X
65	YO2	O		Luminance signal output pin bit 2	X
66	YO3	O		Luminance signal output pin bit 3	X
67	V _{DD}	—		3.3 V power supply	X
68	YO4	O		Luminance signal output pin bit 4	X
69	YO5	O		Luminance signal output pin bit 5	X
70	YO6	O		Luminance signal output pin bit 6	X
71	YO7	O		Luminance signal output pin bit 7 (MSB)	X
72	V _{SS}	—		Ground	X
73	TEST7	I	Schmitt pull-down 50k	Test input pin bit 7 (1: Test mode)	Not used or connected to GND
74	TEST6	I	Schmitt pull-down 50k	Test input pin bit 6 (1: Test mode)	Not used or connected to GND
75	RESET	I	Schmitt	System reset/input pin 0: System reset 1: Operation	X
76	V _{DD}	—		3.3 V power supply	X

No.	Symbol	I/O	Pad Remarks	Pin Description	Termination of unused pin
77	N.C.	—		Unused pin	Not used
78	V _{SS}	—		Ground	X
79	MODE3	I	Schmitt pull-down 50k	Mode setting pin bit 3 (Equivalent to internal register R656I)	Not used or connected to GND
80	MODE4	I	Schmitt pull-down 50k	Mode setting pin bit 4 (Equivalent to internal register DOSEL)	Not used or connected to GND
81	N.C.	—		Unused pin	Not used
82	OE	—	Schmitt pull-down 50k	Output enable input pin	Not used or connected to GND
83	N.C.	—		Unused pin	Not used
84	N.C.	—		Unused pin	Not used
85	N.C.	—		Unused pin	Not used
86	N.C.	—		Unused pin	Not used
87	TEST5	I	Schmitt pull-down 50k	Test input pin bit 5 (1: test mode)	Not used or connected to GND
88	V _{DD}	—		3.3 V power supply	X
89	TEST4	I	Schmitt pull-down 50k	Test input pin bit 4 (1: test mode)	Not used or connected to GND
90	TEST3	I	Schmitt pull-down 50k	Test input pin bit 3 (1: test mode)	Not used or connected to GND
91	TEST2	I	Schmitt pull-down 50k	Test input pin bit 2 (1: test mode)	Not used or connected to GND
92	TEST1	I	Schmitt pull-down 50k	Test input pin bit 1 (1: test mode)	Not used or connected to GND
93	TEST0	I	Schmitt pull-down 50k	Test input pin bit 0 (1: test mode)	Not used or connected to GND
94	N.C.	—		Unused pin	Not used
95	N.C.	—		Unused pin	Not used
96	TESTM	I	Schmitt pull-down 50k	Memory test input pin (1: test mode)	Not used or connected to GND
97	SELF	I	Schmitt pull-down 50k	Self refresh test input setting pin	Not used or connected to GND
98	V _{SS}	—		Ground	X
99	N.C.	—		Unused pin	Not used
100	V _{DD}	—		3.3 V power supply	X

ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.5 to +4.6	V
Input pin voltage	V_I	$T_a = 25^\circ\text{C}$	-0.5 to $V_{DD} + 0.5 \leq 4.6$	V
Output pin short-circuit current	I_{OS}	$T_a = 25^\circ\text{C}$	50	mA
Power dissipation	P_D	$T_a = 25^\circ\text{C}$	1	W
Operating temperature	T_{opr}	—	0 to 70	$^\circ\text{C}$
Storage temperature	T_{stg}	—	-50 to +150	$^\circ\text{C}$

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.0	3.3	3.6	V
Power supply voltage	V_{SS}	0	0	0	V
Operating temperature	T_a	0	—	70	$^\circ\text{C}$

Pin Capacitance $(V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, f = 1 \text{ MHz}, T_a = 25^\circ\text{C})$

Parameter	Symbol	Min.	Max.	Unit
Input capacitance	C_i	—	7	pF
Input/output capacitance (SDA)	C_{io}	—	7	pF
Output capacitance	C_o	—	7	pF

DC Characteristics

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" level input voltage	V _{IH1}	—	V _{DD} × 0.7	V _{DD} +0.3	V
"L" level input voltage	V _{IL1}	—	-0.3	V _{DD} × 0.3	V
"H" level input voltage (TEST1–TEST7, TESTM, SELF)	V _{IH2}	—	V _{DD} × 0.75	V _{DD} +0.3	V
"L" level input voltage (TEST1–TEST7, TESTM, SELF)	V _{IL2}	—	-0.3	V _{DD} × 0.25	V
"H" level input voltage (SDA, SCL, IVS, IHS, <u>RESET</u>)	V _{IH3}	Schmitt	V _{DD} × 0.75	V _{DD} +0.3	V
"L" level input voltage (SDA, SCL, IVS, IHS, <u>RESET</u>)	V _{IL3}	Schmitt	-0.3	V _{DD} × 0.25	V
"H" level input current (pull-down)	I _{IH}	50 kΩ pull down	20	200	μA
Input leakage current	I _{IL}	—	-10	+10	μA
"H" level output voltage (other than SDA)	V _{OH}	I _{OH} = -4 mA	2.4	V _{DD}	V
"L" level output voltage (other than SDA)	V _{OL}	I _{OL} = 4 mA	0	0.4	V
"L" level output voltage (N-Ch. OD) (SDA)	V _{OOL}	I _{OL} = 4 mA	0	0.4	V
Output leakage current	I _{OL}	0 ≤ V _{out} ≤ V _{DD} Output disabled	-10	+10	μA
Supply current (during operation)	I _{DD1}	ICLK: 29.5MHz Output disabled	—	100 (TBD)	mA
Supply current (during standby)	I _{DD2}	Input pin = 0 V	—	5	mA

AC Characteristics

(Ta = 0 to 70°C)

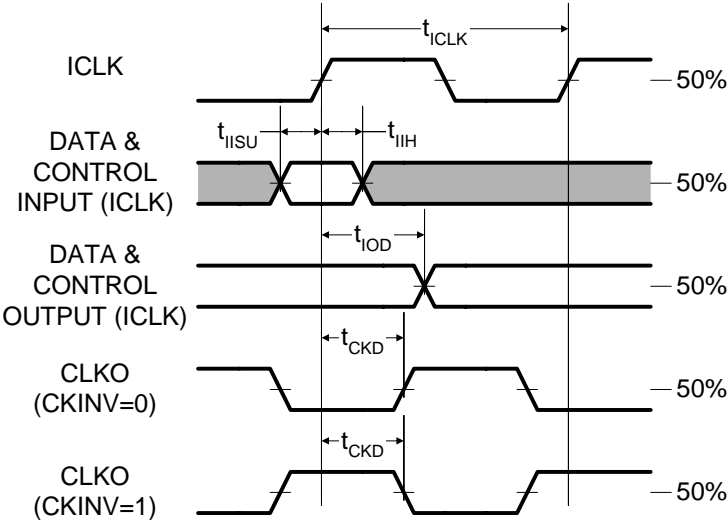
Parameter	Symbol	Condition	Min.	Max.	Unit
ICLK clock cycle time	t _{CLK}	—	33	—	ns
ICLK clock duty ratio	dt _{CLK}	—	40	60	%
ICLK input set-up time	t _{IISU}	—	5	—	ns
ICLK input hold time	t _{IIH}	—	3	—	ns
ICLK output delay time	t _{IOD}	C _L = 30pF	2	25	ns
CLKO delay time	t _{CKD}	C _L = 30 pF (IICLK output)	2	25	ns
		C _L = 30 pF (ICLK output)	2	17	
Data through time	t _{DIDO}	C _L = 30 pF	2	17	ns

Note 1: Measurement conditions

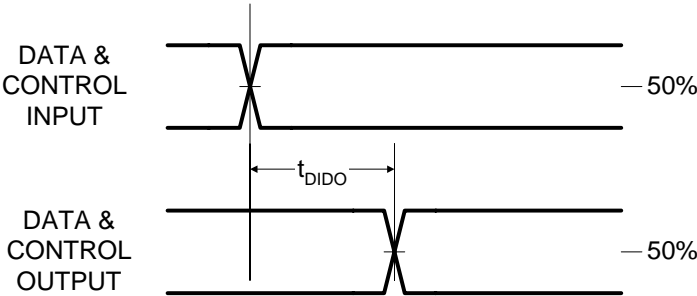
Output comparison level: V_{OH} = V_{DD}/2, V_{OL} = V_{DD}/2Input voltage level: V_{IH} = V_{DD}, V_{IL} = 0.0 VNote 2: Input/output data for the internal memory is guaranteed from the third input-system vertical synchronization signal with RESET = 1 after V_{DD} reaches 3.0 V after the power is turned on. (Due to memory initialization, the first and second data for two fields is not guaranteed.)

INPUT/OUTPUT TIMING

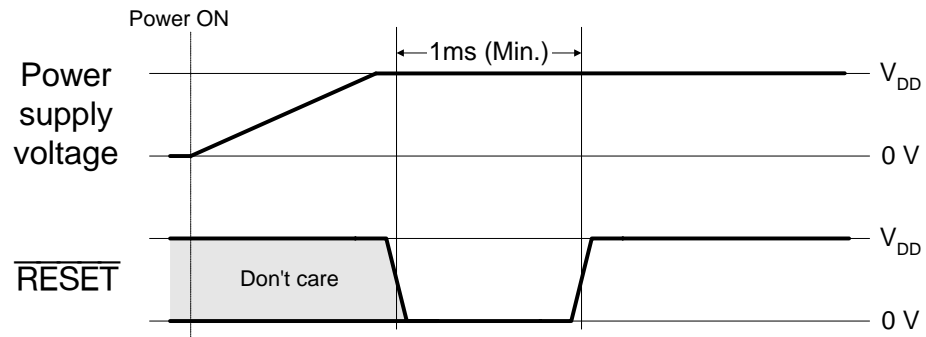
1. ICLK Input/Output Timing



2. Data through Mode Input/Output Timing



3. System Reset Timing



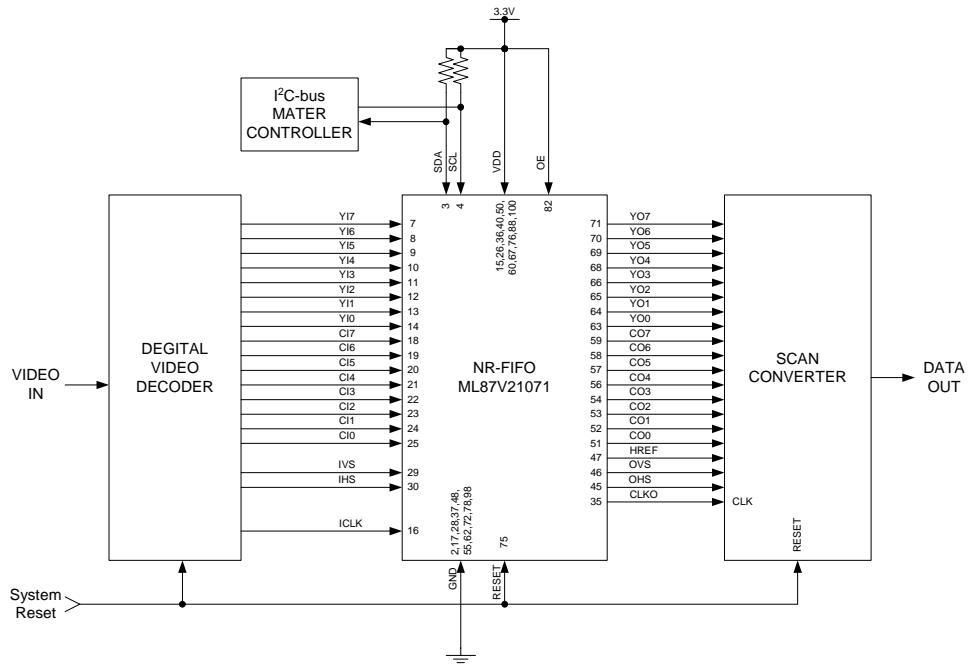
* When the power supply voltage reaches V_{DD} (3.0 to 3.6 V) from 0 V after power is turned on, input 0 to the $\overline{\text{RESET}}$ pin for 1 ms or more to initialize the internal circuits.

* After the $\overline{\text{RESET}}$ pin goes to 1, the I^2C -bus interface can be used while the input of ICLK is stable.

APPLICATION EXAMPLES

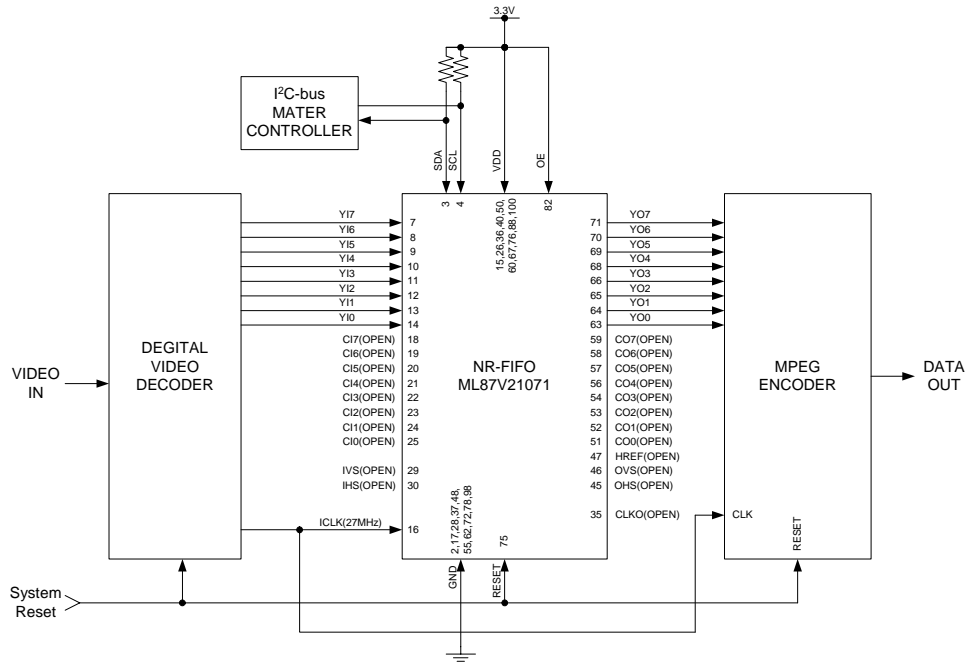
Application Example 1

Mode setting: Open
 Slave address: 1011100
 Input format: 16-bit YCbCr (Register setting: DISEL = 0, R656I = 0, DOSEL = 0)



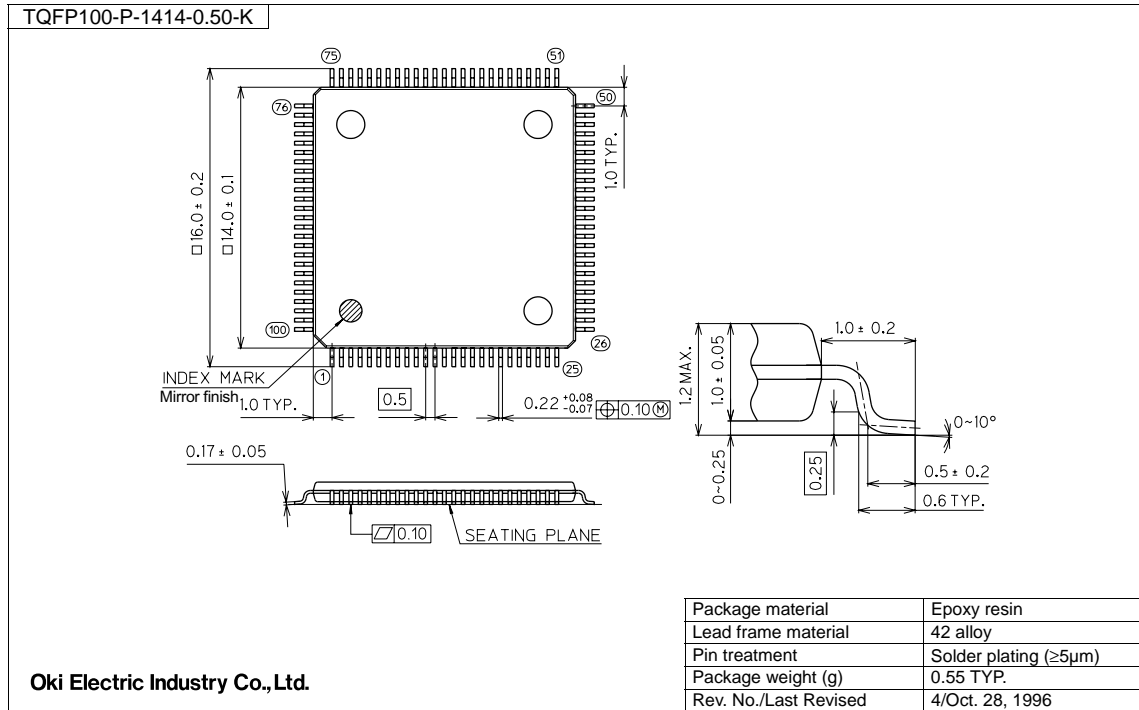
Application Example 2

Mode setting: Open
 Slave address: 1011100
 Input format: ITU-R BT656 (Register setting: DISEL = 0, R656I = 1, DOSEL = 1)



PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL87V21071DIGEST -01	Nov. 15, 2005	–	–	Preliminary edition 1

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